Proving the Absence of Microarchitectural Timing Channels

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Microarchitectural timing channels are a major threat to computer security. A set of OS mechanisms called *time protection* was recently proposed as a principled way of preventing information leakage through such channels and prototyped in the seL4 microkernel. We formalise time protection and the underlying hardware mechanisms in a way that allows linking them to the information-flow proofs that showed the absence of storage channels in seL4.

1 INTRODUCTION

Timing channels bypass the operating system's (OS's) security enforcement by leaking information through the timing of observable events, such as the response time of a server or the observer's own rate of progress. In the case of *microarchitectural* timing channels, this is achieved by manipulating hardware resources, such as caches, TLB, branch predictors and prefetchers, that are abstracted away by the *instruction-set architecture* (ISA) [Ge et al. 2018b].

Like other forms of covert channels, timing channels break *confinement*, the ability to prevent a service from leaking a client's secrets [Lampson 1973]. Confinement is highly desirable whenever sensitive data is processed by an untrusted service, such as a web browser, or any third-party application installed on a computer or mobile device. In principle, any code of sufficient complexity, unless proved correct, must be suspected to contain bugs that can be leveraged by an attacker into Trojans that leak secrets. Furthermore, the Spectre attacks demonstrated the construction of a Trojan from speculatively executed gadgets in innocent code, where the Trojan used timing channels to leak secrets across security boundaries [Kocher et al. 2019].

In practice this means that it is infeasible to rule out the existence of Trojans that leak information via covert channels, and we must instead rely on the OS to enforce sufficient isolation. For *storage channels* this is a solved problem: the seL4 microkernel [Klein et al. 2009] was formally proved to be free of storage channels [Murray et al. 2012]. No such proof exists for *timing-channel freedom*.

However, there is hope: Ge et al. [2019] recently proposed *time protection*, a set of OS mechanisms designed fundamentally to *prevent* all possible leakage through microarchitectural timing channels (hereafter referred to as μ TCs) by making it impossible to pass information through *any* microarchitectural state. These mechanisms included flushing on-core state on domain switch, partitioning the OS's text and stack to occupy distinct per-domain colours in the off-core memory caches, and padding time after flush operations up to their worst-case latency. Ge et al. implemented

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time protection in an experimental version of seL4 that supports only a separation kernel policy, but also observed that – even for this most restrictive of policies – contemporary hardware lacked the mechanisms to enable the OS to completely remove the channels, leaving a degree of vulnerability. More recently however, Wistoff et al. [2021, 2023] added a suitable mechanism to flush all on-core state with time padding up to a specified minimum execution latency, in the form of a new instruction called fence.t, to an open-source RISC-V processor core with minimal increase of implementation complexity and no performance cost, making time protection for on-core μ TCs feasible.

This raises the intriguing possibility of formally *proving* the prevention of leakage through μ TCs. Verification is highly desirable for any code that is critical to security enforcement. It is particularly important for the implementation of time protection, as even logically correct code may lead to observable timing variations. To date, formal reasoning about such timing variations has been considered extremely challenging and generally infeasible.

Heiser et al. [2019] previously proposed that, as μ TCs result from competing access to hardware resources, and time protection strictly partitions all such resources either spatially or temporally [Ge et al. 2019], reasoning about timing channels can be transformed into reasoning about storage channels. However, we have found that making this link *formally*, between reasoning about storage access and their impact on time via the microarchitecture, is highly non-trivial as it still requires reasoning about the *sequence* of accesses to that storage.

Moreover, information-flow properties are notoriously difficult to reconcile with *refinement*, i.e. proofs that a concrete implementation satisfies an abstract specification, as refinement does not generally preserve information flow. Traditionally, that challenge is overcome by removing any observable nondeterminism from the specification, as done in the seL4 information-flow proofs [Murray et al. 2013]. However, this is not possible here, as the exact behaviour of the microarchitecture is unspecified (for good reason). We address this challenge by an over-approximation of accessed storage that supports reasoning about timing channels that is preserved under refinement.

This over-approximation is a significant departure from the existing verification approach of seL4, creating a new challenge of integrating with the a huge, organically grown proof base not designed with such changes in mind (see Section 3.2). In tackling this challenge, we base our work on the original time protection OS mechanisms of [Ge et al. 2019], as reimplemented by us on RISC-V to take advantage of the new fence.t instruction of Wistoff et al. [2021]. This presents a starting point that supports only separation-kernel policies that enforce complete isolation between domains; we found the challenges in integrating time protection into the seL4 proof base even for the separation kernel case to be significant enough that we must consider non–separation-kernel policies as future work.

We make the following contributions:

- a new abstraction of *touched addresses* as an over-approximation of address traces that enables information-flow reasoning (Section 3.1) in a manner we believe is amenable to refinement (Section 6.5);
- a reasoning framework for time protection that utilises the above abstraction, and is *external* to the existing seL4 proof system (Section 4); crucially, this includes a proof that **if** we have a secure system model that tracks the touched addresses, we can produce a proof of time protection for that system, as long as well-defined system and hardware requirements are met;
- a formalisation of the aforementioned hardware requirements the hardware-software contract that supports verification of time protection (Section 5);
- changes to the kernel implementation as a result of our formal reasoning, and a report on our current progress in the repair of the seL4 proofs to return them to a fully-proved state including an investigation of the future work needed to integrate the external time-protection model with the seL4 proofs (Section 6);

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experimental validation that time-protection implementation remains effective despite these changes (Section 7).

Here, as in Ge et al. [2019], we limit our scope to assume a single-core system with no hardware-level multithreading – a necessary limitation for us given that the multicore verification of seL4 is an unfinished area of active research.

2 BACKGROUND

2.1 Covert channels

A *covert channel* is an information flow that uses a mechanism not intended for information transfer [Lampson 1973]. As such it can be used to violate a system's security policy, by leaking information across security boundaries that do not authorise such information flow. Some covert channels may serve as *side channels*, if an attacker is able to extract a secret from a security domain as a side effect of an innocent execution of the domain that holds the secret. In contrast, a covert channel that is not a side channel requires insider help, e.g. a *Trojan* that colludes with the attacker (also referred as a *spy*) to actively leak information. Such a covert channel represents the worst case of leakage, and is what we concern ourselves in this work.

Covert channels are further classified by the mechanisms they exploit. Physical channels, such as temperature [Masti et al. 2015; Murdoch 2006], power draw [Kocher et al. 1999] or electromagnetic [Genkin et al. 2015; Quisquater and Samyde 2001] or acoustic [Backes et al. 2010; Genkin et al. 2014] emanation, generally require physical access or at least proximity, these are out of scope of this work. In contrast, a channel that can be used by a (remotely controlled) unprivileged spy program for unauthorised access to protected secrets is a primary OS concern. Traditionally these are classified as either *storage* or *timing channels*, depending on whether or not their exploitation requires the measurement of timing of events [Department of Defence 1986; Schaefer et al. 1977], although Wray [1991] notes that this distinction is more of an approach to exploitation than fundamental.

Nevertheless, storage channels are considered an easier problem than timing channels, due to the difficulty of reasoning about (or preventing) minor variation in execution timing. Specifically, the information-flow proofs of seL4 [Murray et al. 2013] prove the absence of leakage through storage channels but are quiet on timing channels.

2.2 Microarchitectural timing channels

Timing channels can have various causes, such as data-dependent control flow in crypto algorithms [Molnar et al. 2006]. The OS cannot be held responsible for such algorithmic channels. In contrast, microarchitectural channels exploit hardware resources, and only the OS has full control over hardware and the OS is therefore responsible to closing such channels.

 μ TCs exploit hardware that is functionally transparent and as such mostly or completely abstracted away by the hardware-software contract, the instruction-set architecture (ISA). The purpose of such hardware is improving averagecase performance, which implies that its presence (and state) can be sensed by observing execution speed. Examples are the CPU I- and D-caches, TLBs, branch predictors and prefetchers [Ge et al. 2018b]. These hardware resources hold state that depends on recent execution history and is used to speed up future operations, based on temporal or spatial locality.

Exploiting these channels involves probing the footprint left by past execution on the hardware state. A typical approach is *prime-and-probe* [Osvik et al. 2006; Percival 2005]: The spy *primes* the hardware, e.g. by reading a large enough buffer to ensure that the L1 D-cache only holds spy data. It then waits for the Trojan to execute, leaving its footprint in the cache. The spy then *probes* the cache, again by accessing the large buffer to touch every cache line,

while observing access latencies. Fast access means that the spy's original data is still cached, while slow access means that the corresponding cache line has been replaced by the Trojan, thus conveying information from Trojan to spy. Similarly, the I-cache can be probed by using jumps instead of loads, and the same basic approach can be used to probe the TLB, branch-predictor and prefetcher state.

2.3 Time protection

Ge et al. [2019] proposed time protection (as the temporal equivalent of memory protection) as a principled way of preventing timing channels. They postulate that timing channels are eliminated if all potentially shared hardware resources are either spatially or temporally partitioned.

Spatial partitioning applies to off-core caches, which are physically addressed, and hence can be partitioned by the OS using page colouring [Kessler and Hill 1992; Liedtke et al. 1997; Lynch et al. 1992]: the OS prevents competing accesses to the same cache lines by allocating physical memory so that the cache footprints of different domains cannot overlap.

On-core state is accessed by virtual address, which is out of control of the OS, and therefore must be temporarily partitioned, i.e. securely multiplexed [Ge et al. 2019]. This means that all such hardware resources must be reset to a defined state when handing the hardware to a different security domain.

As temporal partitioning cannot help if hardware is accessed by different security domains concurrently, this means hyperthreading must be disabled or all of a core's hyperthreads must belong to the same domain. Furthermore, as the reset latency may depend on the hardware state (at least in the case of data caches that require writing back dirty data), it must be padded to the worst-case latency to prevent the reset time from becoming a channel.

Colouring *all* memory is challenging, given that the kernel needs to execute instructions and access data. Ge et al. [2019] address this by *cloning* the whole kernel, so each domain has its own kernel image that handles system calls, each with its own text and data sections.

However, there is a small amount of shared global kernel data that cannot be cloned as it is required to coordinate kernels on a domain switch, via whose footprint in the off-core caches Ge et al. [2019] identified the opportunity for an inter-domain timing channel. Ge et al. attempted to make accesses to this data deterministic by pre-fetching it into the caches on a domain switch; in this paper, we instead model the treatment of these accesses via a hardware primitive that allows a targeted flush of this state from the off-core caches, as claimed to be needed by Sison et al. [2023] – we discuss our findings and recommendations for future work on this issue in Section 8.1.

Ge et al. [2019] do not deal with channels resulting from bandwidth-limited shared interconnects [Hu 1991; Wu et al. 2012], and instead assume that all cores are co-scheduled to the same security domain. They also leave channels resulting from off-chip state, such as memory controllers [Deutsch et al. 2022; Wang et al. 2014], out of scope. We limit our scope in the same way, and for now explicitly assume single-core operation.

Within these constraints Ge et al. [2019] demonstrated that time protection can be implemented at low overhead and is largely effective in eliminating timing channels. However, they also found that present main-stream x86 and Arm processors contain microarchitectural state that cannot be reset by any architected mechanism, resulting in residual state (in branch predictors and prefetchers) that the OS is unable to close.

Wistoff et al. [2021, 2023] have meanwhile demonstrated a new instruction, fence.t, that performs a full, deterministic reset of all non-architected state (which they call *microreset*) and enforces a specified minimum execution latency ("time padding"). They implemented fence.t in the Arianne (aka. CVA-6), an open-source RISC-V core. They find

that fence.t eliminates all known μ TCs on their processor. They also show that fence.t is cheap in terms of silicon overhead (0.4%) as well as execution time (no latency added over that of the L1-D-cache flush).

2.4 seL4

seL4 is a microkernel with a comprehensive formal verification story, covering functional correctness of the implementation down to binary code, and proofs that the kernel is able to enforce integrity, availability and confidentiality [Klein et al. 2014]. Originally done for 32-bit Arm processors, the proofs have meanwhile been extended to the 64-bit RISC-V architecture (RV64) [seL4 Foundation 2021]. The information-flow proofs establishing confidentiality exclude storage channels through architected state the kernel is aware of, but explicitly do not address timing channels.

Ge et al. [2019] implemented time protection in an experimental version of seL4, which added kernel cloning. Each thread in the system is associated with a kernel image, and when, during normal execution of the kernel, the scheduler selects a thread bound to a different kernel, the kernel performs the time-protection operations before switching the kernel page-table pointer (which switches the kernel image).

In contrast, seL4's information-flow proofs are based on a *domain scheduler* which implements strict time partitioning (fixed, round-robin time slices for each domain), with a secondary scheduler in each domain responsible for scheduling inside a time partition. Our work aims to leverage the existing information-flow proofs and as such is based on this domain scheduler.

2.5 Refinement

seL4's verification uses refinement [de Roever and Engelhardt 1998]: A concrete model (implementation) is proved to only exhibit a subset of behaviours of an abstract model (specification). In seL4's case there is a hierarchy of models:

- (1) Abstract statements of security enforcement (integrity and confidentiality);
- (2) an access-control model that lumps fine-grained seL4 capabilities into classes of access;
- (3) the (operational) abstract specification of the kernel, describing individual system calls, their arguments and how they act on the state of the abstract system model;
- (4) an executable specification (originally derived from a Haskell implementation);
- (5) the implementation (C code formalised in the theorem prover through a parser written in Isabelle/HOL) [Tuch et al. 2007];
- (6) the executable binary code (formalised through an ISA specification in the HOL4 prover [Fox and Myreen 2010]).

Most of these proofs are performed by interactive theorem proving (ITP) in the Isabelle/HOL proof assistant [Nipkow et al. 2002] (the exception is the last refinement step, which uses an automated tool chain). Confidentiality is proved by formal information-flow reasoning [Murray et al. 2013]. Intuitively, there is no flow of information from a secret-holding "High" domain to another "Low" domain, if Low is not influenced by the state of High. Specifically, assume we compare two execution traces of Low which start from the same global system state, except for the value of a secret held by High. If the two traces are indistinguishable then there is no information flow from High to Low.

An inherent challenge here is that refinement generally does not preserve information flow confinement. To illustrate this, consider a specification that states that a function intended to be a random-number generator returns any integer; the function can be called by anyone without requiring specific privilege. The exact functionality is left unspecified via non-determinism. Any implementation that returns an integer is a refinement of that specification, even if it returns the value of a secret variable, which obviously violates confidentiality.

One way to preserve reasoning about confidentiality through refinement is to make all observable behaviour deterministic in the specification – this is the approach chosen in seL4's confidentiality proofs. However, this is only possible if all information on which decisions are made can be made visible in the specification. This is not always feasible. In particular for our purposes, we will be interested in the sequence of accesses to memory, which in turn determine the impact on the microarchitectural state that causes timing channels. This exact sequence is not necessarily available.

3 TIME-PROTECTION VERIFICATION CHALLENGES

3.1 The unknown-trace problem

As mentioned above, information-flow proofs of confidentiality enforcement reason about execution traces of programs. However, the very nature of the microarchitecture makes it infeasible to have exact traces, and therefore to compare arbitrary traces precisely. This would require a precise model of the microarchitecture, but details of the microarchitecture are intentionally left unspecified by the hardware-software contract, to enable portability of code and retain hardware manufacturers' freedom to optimise. For example, out-of-order processors will reorder instructions, which changes memory-access traces. Similarly, cache-line replacement policies affect cache residency, which also affects memory traces.

Furthermore, even if there was a sufficiently complete model of the hardware to make traces deterministic, this would be far too complex for formal reasoning.

So we have to accept the unknown-trace problem, and thus our inability to reason about precise traces.

We address this by an over-approximation: We replace an exact memory trace by the *touched address* (TA) set, the set of all memory locations that we predict to be *potentially* accessed during the execution of a security domain. Some examples of typical over-approximations in these predictions are (1) including the addresses occupied by the entirety of a given kernel object when only part of it is accessed or (2) including every object in a table when only one of them is accessed. Key to our approach will be that the extent of these overapproximations is irrelevant as long as the proofs maintain the invariant that the TA set remains a subset of the appropriate partition (see Section 4.5, Theorem 4.1). It will then fall within the scope of certain "no-fail" obligations in the refinement proofs (see Section 6.2) to enforce our abstract specification-level assertions that the actual addresses accessed *always* remain a subset of the predicted TA set.

This approach enables us to prove a stronger property than the standard equality of traces: We quantify over *all* traces of interactions with addresses that lie within this over-approximated set – in our model, this will be all sequences of reads, writes, and off-core flushes that impact the microarchitectural state relevant to addresses within that set (see Section 4.2). This in turn supports proving a formal notion of OS-enforced time protection that is meaningful at any level of abstraction of the OS. Furthermore, this formalisation of time protection is compatible with refinement, as it allows reasoning about the impact of each stage of refinement on the TA set.

3.2 Proof reuse

Interactive theorem proving, as used for seL4, is a very labour-intensive process. The total proof base of seL4 by now comprises well over a million lines of proof script [seL4 Foundation 2023], likely the largest interactive bodies of proof

ever constructed. Hence, when attempting to verify any variant of seL4, such as one that supports time protection, the ability to re-use most of the existing proof base is of critical importance.

Predating the concept by over a decade, naturally none of the seL4 specifications or proofs were written with even a *thought* of one day attempting to use them to formalise and prove time protection. Indeed, the seL4 authors initially considered proving absence of timing channels infeasible [Klein et al. 2011].

The upshot is that the changes needed to verify time protection in seL4 must be minimally invasive on the existing proof base. This needs careful proof engineering and is especially true for incorporating the concept of touched addresses, as it alters the essence of the seL4 specifications and proofs: it potentially introduces state change into many parts of the specification that previously were read-only.

In the next section we present an extension model for reasoning about time protection that is separate to the existing seL4 system proofs. We will discuss integration of the models in Section 6.

4 THE TIME PROTECTION EXTENSION

In this section we will discuss the design of an external system model for proving time-protection properties about seL4's abstract specification. First we explain why this external model can guarantee the absence of μ TCs in the host model (i.e. the seL4 model) despite being entirely external to it. We then describe the extension itself and the security property we have proved will hold, as long as certain system and security requirements hold about the original model. We defer a discussion of the hardware assumptions until Section 5.

4.1 Why an extension is sufficient to capture μ TCs

We follow the same justification as Sison et al. [2023] for defining time protection as equivalences on the microarchitectural state abstractions rather than modelling the activity of the spy directly; this allows us to justify modelling the microarchitecture in an extension of the model rather than integrating it directly into the original model.

A high level view of the models in question might look like the following. If we consider the existing system model from seL4's proof base, and describe this as a transition system T_a , this system is aware of what we call *abstract state* – it is not aware of low-level details about hardware, and certainly has no knowledge of microarchitectural state. Our only modification to T_a is to have it track a touched-address set (as described in Section 3.1; details relegated to Section 6).

Although our goal is to reason in detail about microarchitectural state and its interaction with other hardware and time, it is not practical to add that state directly to seL4's proof base (T_a). This would require us to model all of that state's impact on the original state, impacting all existing proofs. As outlined in Section 3.2 we preserve existing proofs by creating an external system model T_μ in which to model microarchitectural state transitions.

In creating this new transition system T_{μ} , we seek to represent real-world flows of information between microarchitectural state and the higher-level hardware state that is represented in seL4's abstract state (hereafter referred to as s_{μ} and s_a respectively). In this conceptualisation, behaviour from a Trojan leaving a fingerprint on s_{μ} is then considered a flow from s_a to s_{μ} , and a spy observing this fingerprint in s_{μ} is considered a flow from s_{μ} to s_a .

With the transitions in T_{μ} modeled from the transitions in T_a , with microarchitectural consequences in s_{μ} following from transformations to s_a , we can faithfully model any information flows caused by the Trojan from s_a to s_{μ} .

In modelling T_{μ} as an extension of T_a , we have chosen not to model the flows induced by the spy back from s_{μ} to s_a ; indeed, with seL4's model T_a never being aware of microarchitectural state, the combined model is not directly able to represent a spy observing microarchitectural state and making decisions based on what is observed.

Instead we argue that, for proving the absence of μ TCs, it is sufficient to prove that any microarchitectural state accessible to a spy contains no secrets while the spy is executing; this is because any spy-induced flow of information from s_{μ} back to s_a must follow from information already in s_{μ} , which is thus capturable by an information-flow property on T_{μ} .

4.2 The model of microarchitectural state

We achieve the above aim by adapting the methods presented by Sison et al. [2023]: include *flushable state*, *partitionable state*, and *time* in s_{μ} . From here on we use the term *flushable* to refer to *temporally partitionable* state, and refer to spatially partitionable state as simply *partitionable*.

We enumerate different low-level hardware interaction units, and model how these interactions affect microarchitectural state:

- **Reads:** given some (virtual and physical) address, a memory read operation will have some underdefined impact on the flushable state, and will impact any relevant areas of the partitionable state. For example with coloured off-core caches, this will have an impact on the current colour of the L2 cache.
- Writes: these will have similarly undefined impacts on both the flushable and partitionable states. The in-model behaviours of read and write impacts on the microarchitectural are implemented identically, but are separated so that somebody using this model could represent the different microarchitectural effects of read and write operations.
- **On-core flush:** represents the fence.t primitive presented in Wistoff et al. [2021], which in our model returns all flushable state to a predefined value.
- **Targeted off-core flush:** allows some section of the partitionable state to be flushed. The semantics here return some parts of the partitionable state to a predefined value, specifically the state relating to some set of addresses provided, as well as any addresses deemed to *collide* in the partitionable state (i.e. addresses that map to the same cache set). This would flush the entire cache sets that may hold data addressed by a particular physical addresses.
- **Pad to time:** simply advances the time to a given constant, assuming it is in the future. This represents a hardware padding operation, and does not have any impact on flushable or partitionable microarchitectural state, apart from the clock itself.

The operations for reading, writing, and targeted off-core flushing are all parameterised by addresses (both virtual and physical). We consider an operation to *adhere to* a touched addresses set if the address(es) used by the operation are contained within the touched addresses set. We consider a full hardware interaction trace to be a sequence of these operations, and we consider a trace to adhere to a touched addresses set if all of its component operations adhere.

To model the microarchitectural transformations associated with an abstract state transition t_a in T_a , we choose a trace that adheres to the touched addresses set associated with t_a . We assume an underdefined *trace selector* function that, given a touched addresses set, produces some hardware interaction trace that adheres to the set. For example, if the TA set is $\{1, 2\}$ the selector may return [Read 1, Write 2, OffCoreFlush $\{1, 2\}$, OnCoreFlush, Pad t], or its reorderings or extensions swapping any of the addresses with anything in $\{1, 2\}$ and any time t.

Given that our proofs have no knowledge of which trace is selected, except that we know that the selected trace adheres to the touched addresses set, our proofs must allow that any possible trace could be selected, effectively quantifying over all possible traces.

Although we quantify over all traces whose accesses stay in the TA set, we place a crucial *dependency* restriction on the underdefined trace selector function: the trace it selects must depend only on microarchitectural state *visible* to the appropriate observer during a particular transition. Consider the following example, in which a system contains two security domains A and B. At any given time, either A or B is the currently-executing domain – when the kernel is executing, it is either doing so on behalf of one of these domains, or it is performing a domain-switch between these domains.

During some transition t_b , if *B* is the currently-executing domain, then from the perspective of *A*, the transition could branch on any number of secrets belonging to *B*, so we have no idea what their trace will look like. We assume that t_b will encode secrets in all of the flushable state, as well as any of the partitionable state allowed by the transition's touched addresses set. We know nothing about the time at the start or end of this transition. To know that no secrets are learned by *A*, we need to know that *A* cannot observe any of the microarchitectural state affected by this transition. We consider *A* (as a non-executing domain) to be able to observe only the parts of partitionable state that are assigned to *A*, excluding parts of this state that can be affected by kernel global data (which *B*'s transitions could impact). We therefore only need to know that *B*'s touched addresses set contains no addresses in *A*'s partition of the partitionable state, except for those in the kernel global data.

From the perspective of *B*, however, the flushable state is considered observable, as well as *B*'s partition of the partitionable state, *and* any part of the partitionable state affected by kernel global data. So, from *B*'s perspective, the transition t_b will affect plenty of visible microarchitectural state. To preserve confidentiality in this instance, we need to know that the details of the transition are not dependent on any of *A*'s secrets. In particular, aside from the kernel global data, we know the transition will only affect parts of *B*'s partitionable state, as the traces will be induced from a TA set relevant to addresses wholly within *B*'s partition; however, we still need to know that the *choice* of how that state is affected – for example, the order of *B*'s sequence of accesses to its own partition – is not affected by any secrets from *A*. To enforce this, we only need to know that the trace selector function did not consider any of *A*'s secrets when choosing a particular hardware interaction trace to return.

This boils down to the following assertion: the trace selector function can only consider microarchitectural state visible to the *currently-executing* domain when making its decision on which adherent trace to select. In real-world terms, this means that we are assuming that during some execution, the hardware trace is only affected by microarchitectural state that is modeled as visible to the currently-executing domain. This means we must carefully choose our definition of *observable* to accurately reflect reality.

We define the parts of microarchitectural state observable to the currently-executing domain to be:

- the entirety of the flushable state;
- the portion of the partitionable state assigned to the observing domain, plus
- any parts of the partitionable state colliding with kernel global data;
- the exact wall-clock time.

Therefore, the only parts of the state that the trace selector *cannot* consider when selecting a trace are the parts of the partitionable state that are assigned to other domains *and* not colliding with kernel global data addresses. Effectively, this formalisation leans on *hardware partitioning* being correctly enforced by hardware – in terms of memory caches, this means that off-core caches must be correctly coloured. As long as this partitioning is correctly implemented, we can prove the absence of μ TCs, when appropriate time protection measures are implemented.

4.3 Time protection measures in the model

As in previous work [Sison et al. 2023], the time protection mechanisms we model are as follows.

- Correctly partitioning the partitionable state.
- Flushing the flushable state during a domain-switch. This models a flush of the entirety of *all on-core microar-chitectural state*, which we consider infeasible to partition including the L1-D/I caches, TLBs and branch predictors. Note in particular this is not just restricted to state relevant to addresses in the TA set.
- Selectively flushing parts of the partitionable cache during domain-switch. This is used to model the flushing of (statically determined) addresses of kernel global data from the *off-core* i.e. L2 cache (and L3, if it exists). Note this is only relevant to the TA set to the extent that we automatically include those globals in the TA set.
- Padding the domain-switch sequence to an appropriate worst-case execution time (WCET).

The model described in this section allows for the flow of secrets into the flushable state (for example on-core caches), but these secrets are removed by a flush before execution is passed to any other domain. The model allows for the flow of secrets into some portions of the partitionable state belonging to other domains (for example off-core caches, via kernel global data), but this section of the partitionable state is also flushed before execution is passed to any other domain. The model allows for the flow of secrets into the rest of the currently-executing domain's portion of the partitionable state, but this state is never observable by another domain. Finally, the model allows for the flow of secrets into the clock itself, as the amount of time taken for a domain-switch sequence to complete can be dependent upon domain secrets, but these secrets are removed when the clock is padded to a domain-switch WCET.

To facilitate proofs for all of the above, we require only that the following property of the touched addresses set holds for every transition: *The touched addresses set for each transition contains no addresses outside of the currently-executing domain's portion of the partitionable state, except for addresses affected by kernel global data.* For all kernel models that meet these requirements, the above claims are formally verified in Isabelle/HOL.

4.4 Enforcing the presence of the time protection mechanisms

Thus far we have discussed how to examine effects on the microarchitectural state that become the medium for μ TCs. There is also the question of how to prove that time protection mechanisms are properly implemented.

When working with an abstract specification that has no knowledge of microarchitectural state, there is no way to examine the semantics of the model to ensure that it is performing time protection strategies in the right way or at the right times.

Instead, we ask the user of our model to specify which specific transitions implement time protection mechanisms, and our microarchitectural model then simulates these mechanisms by executing the primitive flushing and padding operations that make up the time protection implementation.

Specifically we request that a transition that is identified as a domain-switch transition to be separable into four subtransitions: an *old clean* transition, an optional *dirty* transition, a *mechanism* transition, and a *new clean* transition.

- The *old clean* sub-transition needs to meet the same transition requirements as any other transition in the system, via its touched addresses set.
- The *dirty* sub-transition (not used in our integration with seL4) might access addresses belonging to both the *previous* and *next* domains (and therefore affect partitionable state belonging to both), but must have a hardware trace that is determinised only by information known to both the previous and next domains.

- The *mechanism* sub-transition must *only* perform a specific set of primitive microarchitectural operations: flushing of the on-core caches, any targeted flushing of off-core caches, and padding to a set time.
- The *new clean* sub-transition is similar to the *old clean* transition, but is now considered to be operating under the new domain's execution, so must only access addresses belonging to the new domain and in a sequence decided only by secrets visible to the new domain.

Our model executes all transitions as described above, and we then prove that a confidentiality property capturing time protection holds of this model as follows.

4.5 Time protection property of extension

First, we define the TA set to be the union of all virtual addresses associated with all *user-controlled kernel objects* – those allocated by a user program by retyping untyped memory – that the kernel has retrieved so far since the last domain switch, as tracked by calls to the seL4 abstract specification's internal get-object function.

Our new time-protection-relevant proofs, of (1) information-flow security and (2) refinement, need to refer to the TA set. We therefore add it as a *ghost state* field in the seL4 abstract specification – that is, state that is intended to assist proofs but that should not impact the functional semantics of the actual system. (We discuss the mechanics of ensuring the TA set consequently does not impact proof reuse further in Section 6.1.)

In the seL4 information-flow security proofs, we can compare the values in the TA set with policy information determining which kernel resources belong to which domains. For seL4, we lean on an existing invariant proved about seL4 that the page table maintains the mappings to all user-controlled kernel objects at all times, regardless of which domain they belong to, and that these will be unaffected by a domain switch. Thus, to ensure kernel accesses impact only the desired parts of the partitionable microarchitectural state, which is indexed by physical – not virtual – address, we must assert the kernel maintains the following invariant:

PROPOSITION 4.1 (PARTITION SUBSET INVARIANT). The physical translations of all addresses in the TA set, according to the page table, form a subset of the union of physical addresses that reside in the currently running user domain's partition.

The main theorem we have proved of the system extension is as follows:

THEOREM 4.2 (TIME-PROTECTION EXTENSION PRESERVES CONFIDENTIALITY). If confidentiality-u holds for some transition system that consists only of sequences of (1) operations that obey the partition subset invariant and (2) a correctly implemented domain switch sequence, then confidentiality-u_µ holds of its time-protection extension.

Here, confidentiality-u applied to the original system is a version of seL4's original confidentiality property [Murray et al. 2013] modified to enforce an extra equivalence between the values of the TA set; note this constitutes an extra security proof obligation for seL4. Then, confidentiality- u_{μ} as applied to the extended system is the same but extended to assert extra equivalences to *enforce no secrets flow into microarchitectural state fields observable to the currently executing domain* as specified at the end of Section 4.2.

5 HARDWARE REQUIREMENTS

The key hardware features necessary, as laid out by Sison et al. [2023], are that primitives exist for flushing the on-core caches, that the off-core caches are partitionable through cache colouring, and finally that a primitive exists for waiting until a deterministic amount of time until after the arrival of the timer interrupt that triggers domain-switch. These now exist in the form of the fence.t instruction on the CVA-6 RISC-V core [Wistoff et al. 2021, 2023].

Ge et al. [2019] used pre-fetching of shared kernel data to give it a deterministic cache state, which we find to be insufficient and we would need to flush any shared kernel data from the cache completely (see Section 8.1). In order to avoid the prohibitive cost of a full cache flush, this would require a per-address flush primitive.

However, with time protection tied to seL4's domain scheduler, practically all of Ge et al.'s shared kernel data can be partitioned, and the tiny remainder (a link to the next domain to be scheduled) is accessed deterministically, so this complication can be completely avoided (for now, at least).

We obviously require that any flush operations used have a known WCET. Moreover, we require that the hardware's timing behaviour is reliable enough to establish the WCET of any interrupt or system call triggered just before the timer interrupt that triggers the domain switch. Note that Ge et al. [2019] defer operations that occur within a short window before the timer tick until the domain is scheduled next.

We improve on the model of Sison et al. [2023] by allowing the "cachedness" of a given address in the microarchitecture to be expressed as more than just a boolean ("is resident" vs "is not resident"), to allow for data to be cached at different levels in the cache hierarchy.

Moreover, we have discovered a number of requirements not previously described in Sison et al. [2023], that more precisely express on which parts of the microarchitecture the running time of these operations depends. For example, we formalise that the time taken by an on-core microarchitectural flush depends only on other on-core microarchitectural state; moreover, we require that the time taken by the flush of an address from an off-core cache depends only of the cachedness state in that cache of other addresses of that *colour* – the set of addresses whose bits in the overlap of the cache index bits and page bits share a common value. In a similar vein, we require that the access time to a particular address as determined by the off-core cache should depend only on the cachedness state of addresses in its *collision set*. i.e. the set of addresses that compete for the same cache space.

6 INTEGRATION WITH SEL4

The existing proof base for seL4's security and functional correctness proofs is a significant piece of engineering. Here we explain how we implement the touched-addresses abstraction so as to minimise the impacts on seL4's existing proofs; we then discuss this impact. We then describe changes we made to the design of the kernel's implementation of time protection both enabled by, and to facilitate, our formal reasoning. Finally, we explain how we expect our abstractions to enable seL4's refinement to be extended to make the preservation of a time protection property possible.

6.1 Minimising the proof impact

A significant portion of seL4's functional correctness proofs relies on identifying sections of kernel execution that have no impact on the model's state; this is critical to allow the application of proof rules to be reordered or manipulated in various ways. This could include lengthy sequences of complex executions, as long as memory is only read, and never written to (or written to, but without changing values).

Unfortunately, the tracking of touched addresses still constitutes an update to the model state on every mere memory access. To overcome this problem, we adapt the former "no effect on state" characterisation of executions to express "no effect on state other than the TA set", allowing reuse of the many existing proofs that have nothing to do with the TA set.

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6.2 Ensuring TA tracking is comprehensive

To guarantee that accesses are adequately tracked by the TA set, we leverage the failure-tracking mechanisms of the state transformation monads used to model seL4's formal semantics: We model memory accesses (including reads) to *fail* if attempting to access any address that is not already present in the state's touched-addresses set. As long as the TA set has no way of losing addresses during a transition, we can examine the touched addresses set at the end of that transition to gain an upper bound on the set of addresses accessed during the transaction.

There are a few things to note here. Firstly, how do we know that executions do not fail? This is achieved in the existing proof base during refinement, and is not a section of the proofs that we have done significant work in updating. We do know that once "no-fail" in refinement is proved, that our TA abstraction will have been adhered to.

Note further that, at seL4's abstract specification level, we are only able to track addresses this way and enforce that all accesses conform to that tracking (through subsequent "no-fail" proofs) for user-controlled kernel objects. As the kernel's non-user-controlled *global* variables are only assigned addresses further down in seL4's refinement stack, we exclude these from our reasoning at the abstract specification level. We plan to include all addresses in the TA set automatically as they are added to the model by each refinement step, to force a proper treatment of their cache impacts, e.g. by a targeted flush of their addresses from off-core caches.

An important question to ask is: when do we ever remove addresses from the touched addresses set? The important property this set requires is that no addresses are removed from it *during the transition being examined*, if we want to reason about that transition's hardware interaction trace. Therefore it would be safe for the touched addresses set to be emptied *between* or *immediately at the beginning of* each state transition that is being modeled for time protection purposes (i.e. it would be fine to empty the set at every kernel entry or exit point in the seL4 kernel model). In practice, we only empty the touched addresses set in our model during a domain-switch sequence, just as the cache flushes are performed. This point is in the "middle" of a transition as modeled by seL4's view of the domain-switch transition, but between two sub-transitions as modeled by the extension.

6.3 Other impacts on the proof base

Even after careful planning to minimise its impact, adding touched-addresses tracking to seL4's abstract specification required essential utility functions and state accessors to be modified, creating a significant amount of work in returning the proof base to a fully-proved state. Here we will enumerate the various parts of the proof base that are affected, our plan to make these repairs, and how far along we are at time of writing.

Repairing the **abstract invariant** / **functional correctness** proof base is the most significant piece of engineering required after introducing TA tracking to seL4. This is a very large proof artifact, and includes hundreds of lemmas that depend on executions not to make any changes to the state, a property which is broken at every point we add to the touched addresses set. To assist in repairing these proofs, we developed systems that identify various functions that do not make any changes to the state *except for* changes to the touched addresses set, as well as identifying properties/invariants that are not concerned with the contents of the touched addresses set (which we name *TA agnostic* properties), and structures that will discharge proofs about a TA-agnostic property being upheld by a function that changes nothing but the touched addresses set.

The next most difficult repair to the proof base will be in the **refinement** proofs. Fixing this proof base will require showing that each memory access in seL4's abstract specification accesses an address that was previously added to the TA set. At time of writing, we have not made significant progress on repairing these proofs.

Another property required by the external model is that the TA set be equivalent when observed by the domain that is executing. This requires some modifications to the unwinding relation in the **information flow** proof module, as well as updating associated proofs.

Finally, the external time protection model requires that the host system's scheduler meet certain requirements. Aligning these with seL4's domain scheduler will be straightforward with the addition of these requirements to the abstract specification, e.g. that each domain be assigned adequate time to leave room for time protection WCET padding operations.

6.4 Impacts on the kernel design

Our port of seL4's time protection mechanisms to RISC-V also differs from their initial, unverified implementations for ARM and x86 [Ge et al. 2019] to make them more amenable to verification; some of these code simplifications were found to be possible through our formal reasoning. Our empirical results show that these changes make no difference to their effectiveness (see Section 7).

For instance, we reasoned we can invoke microarchitectural flushes earlier on during the domain-switch process, instead of deferring them until just before returning to the user, as a code audit shows that all addresses touched after that point belong to the new domain, and thus make no difference to the provability of the time protection property.

As for changes that simplify verification, we have reduced the number of kernel API changes needed by initialising kernel image clones at boot time according to a static configuration, instead of making them the responsibility of the initial user thread as was done by Ge et al. [2019]. Finally, we found that while Ge et al. copied the kernel stack between images on each domain switch, this is redundant as the stack content is deterministic at this point. This obviates the need for reasoning about the "dirty" sub-transition of the time protection mechanism sequence mentioned in Section 4.4.

6.5 Directions for refinement

We now turn to the question of proving time protection for seL4's C and binary semantics, which are both related to its abstract specification by refinement composed of two successive steps (abstract to C [Klein et al. 2009], then C to binary [Sewell et al. 2013]).

In these refinement steps we will discover whether we predicted all touched memory locations correctly. For refinement to hold, the TA set of a lower level must be a subset of those predicted in the abstract specification. If during the proof we find that they are not, they will have to be added in the abstract specification and the information-flow theorem will have to be re-proved. Furthermore, domain switch sequences will be composed of invocations of the machine specification, which remains the same between all three levels. Therefore we expect to prove the following:

PROPOSITION 6.1 (SeL4 REFINEMENT PRESERVES PARTITION SUBSET INVARIANT AND DOMAIN SWITCH SEQUENCES). Since refinement preserves all invariants, it trivially also preserves the partition subset invariant wherever it originally held. It leaves domain switch sequences unmodified.

Note, that seL4's semantics, that is proved preserved by refinement between all three levels, excludes the precise memory interaction order. This remains appropriate for the C semantics because the C compiler used to compile it to binary is always liable to introduce reorderings of accesses to memory. Nevertheless, as Proposition 6.1 would give us that refinement also preserves the information flow statement, we expect to obtain the best time protection argument we can hope to apply soundly at the C level:



Fig. 1. Channel matrices for kernel-text channel (100,000 samples).

PROPOSITION 6.2 (SeL4 REFINEMENT TO C PRESERVES TIME PROTECTION). If confidentiality-u holds for the seL4 abstract specification then confidentiality-u_{μ C} holds for the time-protection extension of its C semantics.

Here, confidentiality- $u_{\mu C}$ is a time protection property like confidentiality- u_{μ} but suitably adapted to the C specification-level state.

7 EMPIRICAL MEASUREMENTS

Our work uses the FPGA-based CVA-6 core with the fence.t instruction of Wistoff et al. [2023]. Consequently, measurements of channel capacity show the same results, indicating that all measured channels are closed.

The one significant difference in setup to this earlier work is that Wistoff et al. uses the dynamically cloned kernel of Ge et al. [2019], while we use a static, two-kernel configuration, where kernels are switched at the time of the domain switch of the time-partitioning *domain scheduler* of Murray et al. [2013]. To demonstrate that this setup does the job, we repeat the attack the separate kernel images are designed to prevent: the timing channel through the kernel's code footprint in the last-level cache. Specifically, the Trojan does nothing to send a value of 0, or executes a specific system call to send a 1. The spy measures the latency of executing the same system call.

Figure 1a shows the channel matrix (distribution of latencies measured by the spy as a function of the data sent by the Trojan) if both domains share a kernel image. The distributions clearly differ, and we measure a small but significant channel capacity of M = 9.6 millibits (mb). The 95% confidence interval of the apparent channel resulting from statistical sampling error, \mathcal{M}_0 [Ge et al. 2019] is 0.1 mb in this case, which indicates that the result is statistically significant.

With separate kernel images, we get $M = M_0 = 0.1$ mb, indicating the channel is closed. The channel matrix, shown in 1b, shows random fluctuations around the same mean.

8 DISCUSSION / LESSONS LEARNED

8.1 On the effectiveness of determinising the cachedness of kernel global data

Ge et al. [2019] identified a channel via kernel global data. Some kernel global data cannot be cloned, and its footprint in the off-core caches therefore presented the opportunity for an inter-domain timing channel. The authors claimed to patch this channel by determinising the cachedness of these addresses through *prefetching* – that is, by accessing all of them sequentially during a domain-switch.

While examining the details of this countermeasure for formal verification, we discovered that such an approach does not, in fact, put the cache state belonging to this set of addresses into a deterministic state. In fact, without having reliable formal semantics for the specific cache eviction strategies implemented in particular hardware (generally unavailable for modern hardware) we concluded that no set of normal memory interactions can reliably determinise the cache state for any address or set of addresses.

Sison et al. [2023] claimed that such a channel could only be mitigated by a hardware primitive that meets the explicit requirement of determinising such state. We have formalised this in our time protection models, and propose that an off-core cache flushing primitive by address or cache set that reliably resets any additional state influencing the cache's replacement policy would be sufficient.

However, on more detailed investigation we now believe that that shared kernel globals can be reduced to deterministically accessed public data – e.g. domain scheduling data, which can be accessed by no syscalls and is only accessed during the domain-switch sequence and always in the same order. We believe this would obviate the need for determinising the cachedness of that data using either previous methods (prefetch) or a targeted off-core flush; however, we have the formal means of reasoning about such measures if future versions of the kernel render them necessary.

8.2 On extending this model to consider other kinds of microarchitectural state

From our experience in successfully reducing the capture of microarchitectural state changes to the collection of the TA set, we learned that we only need to extract interaction data from the host model at a granularity matching that of the channel elimination strategy: we do not require any knowledge about accesses to on-core caches because they are always flushed anyway, and we only need to know about which partition is accessed by each transition.

We see this as a lesson we can apply in future if we must extend our model to any other stateful microarchitectural feature that is not interacted with via memory accesses, but still can affect the timing of executions. Such a feature would not be represented in our existing microarchitectural model, as the TA set would contain no information about accesses to this feature. However, the approach we have taken thus far in modeling features would make such an adaptation relatively painless; again, we would take the approach of only extracting just enough interaction data from the host model (in this case the seL4 abstract specification) at a granularity to match that of the protection mechanism:

- A feature whose state is fully flushed on every domain-switch could be considered part of the *flushable state*, and no interaction details are needed; the model could quantify over all possible modifications to the feature's state, and as long as a flush operation is available and called alongside existing flushing mechanisms, our model will show that no information can be transmitted via that channel.
- If the feature's state could be partitioned, it would be considered part of the *partitionable state*, and we would only need to extract enough interaction data from the model to know that accesses are to the appropriate partition.

Robust time protection at the OS level will always require some heavy-handed reset operation, as a surgical bit-by-bit cleansing of microarchitectural state will be intractable. The upside of this is that formal reasoning about time protection at the operating system level is also free of bit-by-bit complications, and is satisfied with input data at the same coarse granularity as the elimination strategy.

8.3 On how to handle cross-domain Notifications

So far we have only described a system configured as a separation kernel, where no two domains have any allowed communication channels between them. The next step is to model, and show the absence of timing channels in, a system where some domains can communicate with each other through explicitly allowed channels. These explicit channels are not necessarily bidirectional; some domain *A* may be able to send messages to *B*, but the policy does not allow any information to flow from *B* to *A* (i.e. $A \rightsquigarrow B$ but $B \nleftrightarrow A$). An example of this would be Notifications – a fast and simple one-way cross-domain communication in seL4.

In existing seL4 implementations, if user *A* sends a notification to user *B*, this will involve the kernel writing to parts of *B*'s memory, an operation that might be faster or slower depending on the state of *B*'s partitioned microarchitecture. Thus, the time taken for *A* to *send* a notification will yield secrets about *B*, causing a *backflow* from *B* to *A* that we must eliminate if the information-flow policy disallows it.

Further to this off-core timing channel, there are secrets in *B* that will affect which memory addresses will be accessed while "writing" this notification, and thereby impact on the non-partitioned on-core cache. Therefore, simply padding the "send" time to some WCET will not eliminate the channel, as the on-core cache will reveal secrets about *B*'s readiness to receive a message.

To facilitate the extra channel elimination strategies needed, we anticipate that such cross-domain notifications will need to be added as a separate kernel API to seL4's existing notifications to avoid negatively impacting the latter's performance. Moreover, we expect their verification approach to involve development of a more sophisticated variant of the "dirty" transition that is currently an optional step in our time protection sequence model of Section 4.4.

9 RELATED WORK

Ge et al. [2018a] analysed hardware mechanisms for preventing μ TCs and found that there was insufficient support on contemporary x86 and Arm hardware, leading to a call for an improved hardware-software contract, specifically the requirement for all non-partitionable state to be flushable. Wistoff et al. [2023] propose the fence.t instruction which performs a flush of all on-core microarchitectural state, by resetting all registers that are not explicitly part of architected state. Bourgeat et al. [2019] propose a purge instruction that flushes on-core microarchitectural components to secure enclaves, a similar proposal is the FenceX instruction proposed by Li et al. [2020].

Escouteloup et al. [2021] propose an alternative design that introduces *Dome IDs*, representing security domains. Microarchitectural state is implicitly flushed when changing the current Dome ID. This proposal is presently under discussion in the RISC-V Microarchitecture Side Channels Special Interest Group [RISC-V International 2023]. Our approach, presently based on fence.t, can readily adapt to such an alternative.

Several proposals have been made to partition L1 caches [Dessouky et al. 2021; Domnitser et al. 2012; Page 2005; Percival 2005], while Wang and Lee [2007, 2008] proposed support for locking cache lines. Such approaches do not scale to all microarchitectural channels, except in the extreme case of replicating all state, which would essentially replicate the core.

The use of multiple kernel images has in the past been proposed for improving scalability on multicore platforms [Baumann et al. 2009; Boyd-Wickizer et al. 2008; Nightingale et al. 2009] or hot-plugging of CPU cores [Zellweger et al. 2014]. Ge et al. [2019] proposed per-domain kernel images for preventing cache channels through shared kernel text or data. While their model provides dynamic cloning of a kernel, we replicate at system initialisation time, and statically associate a separate kernel image with each security domain of seL4's *domain scheduler* configuration [Murray et al. 2013].

Prior proofs of OS-enforced confidentiality [Costanzo et al. 2016; Li et al. 2021; Murray et al. 2013] only deal with storage channels through architected state. Barthe et al. [2012] prove elimination of cache-based timing channels through a full cache flush; this approach is prohibitively expensive [Ge et al. 2019]. stealthMem, which reserves some cache colours for safe cryptographic operations, was verified to prevent side-channel leakage [Barthe et al. 2014; Kim et al. 2012] but cannot protect against a Trojan accessing other (non-"stealth") memory areas. To our knowledge, the only prior formalisation of OS security to deal simultaneously with both partitionable and flushable state, as required by time protection, is the prior formalisation of time protection by Sison et al. [2023], on which ours is based.

Finally, Liu et al. [2019] prove a notion of temporal integrity they call *temporal isolation* in a real-time extension of mCertiKOS, but their approach concerns the elimination of storage channels via scheduling state and does not attempt to prevent microarchitectural timing channels.

10 CONCLUSIONS

We have reduced the unknown problem of time protection enforcement by OS kernels to the more familiar verification problem of collecting a set of touched addresses, proving a small number of new invariants on that set and preserving them over refinement.

To this end, we contribute new principles to enable proofs of time-protection properties and their refinement at different levels of abstraction of an OS kernel specification.

We provide an approach for extending existing OS security models to account adequately for time protection. The key conceptual contribution here is the tracking of touched addresses and the use of the extension of that tracking in a way that solves the unknown-trace problem.

For these extensions we provide conditional proof that, given a proof of the the original model's security with the tracking added, yields a proof that its extension satisfies a security property that enforces time protection.

This applies to any OS kernel that satisfies the requirements.

While this proof depends on a conditional statement, there is the following evidence that the assurance of time protection by the seL4 kernel has already increased:

- (1) We provide a complete specification of what is necessary to prove it.
- (2) We have made changes to the kernel implementation based on this specification.
- (3) Our measurements agree with formal predictions.

In doing so, we clarify the required hardware-software contract with respect to previous formalisations of time protection.

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