



School of Computer Science & Engineering
Trustworthy Systems Group

Two interfaces for seL4 kernel verification: Time Protection and the Kernel–Userland Gap

Isabelle Workshop, Jul'26, Lisbon

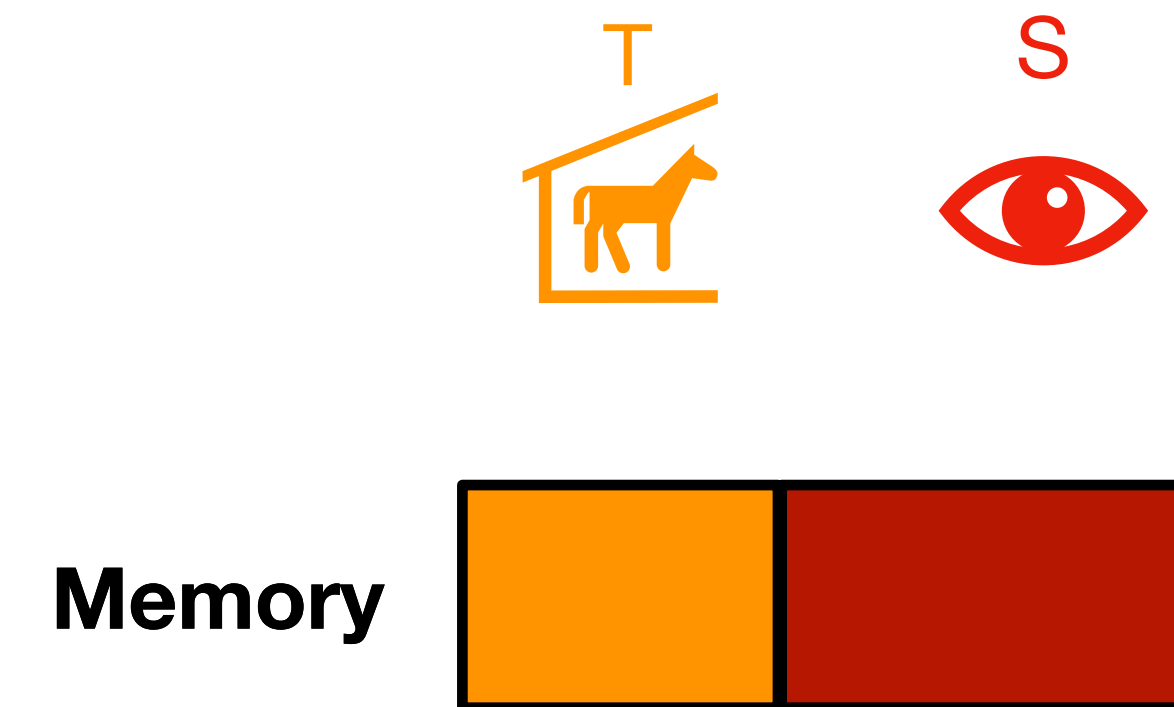
Dr Rob Sison

Senior Research Associate, UNSW Sydney
r.sison@unsw.edu.au



I: Time Protection

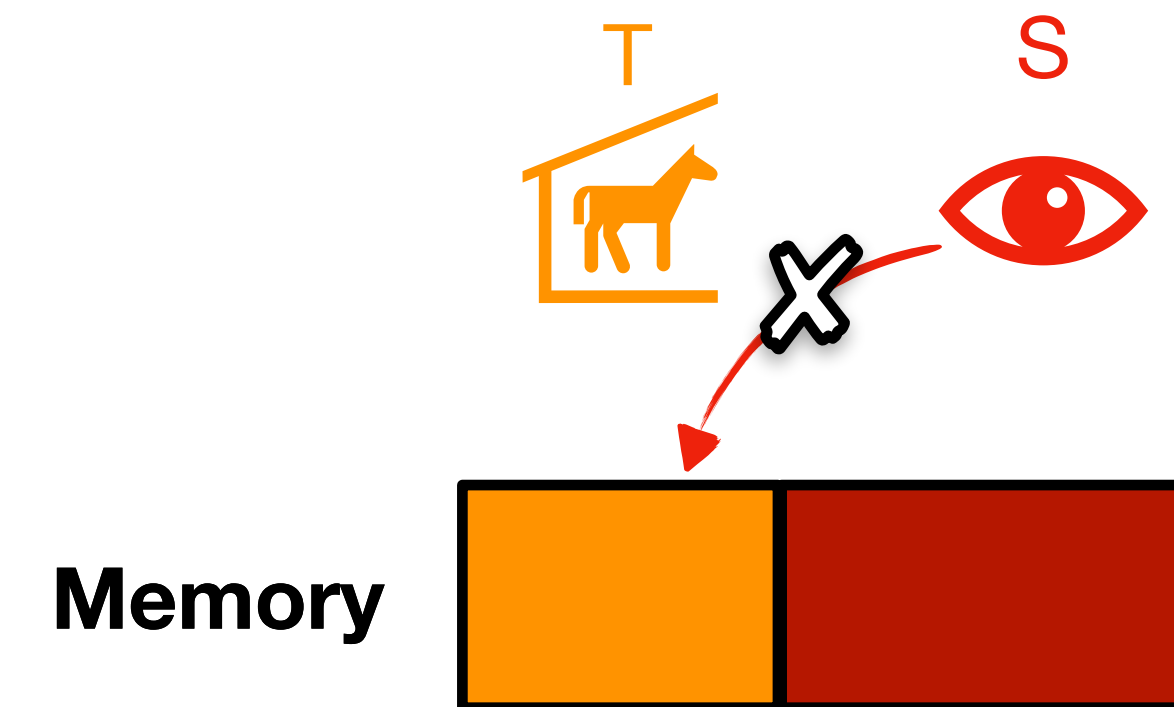
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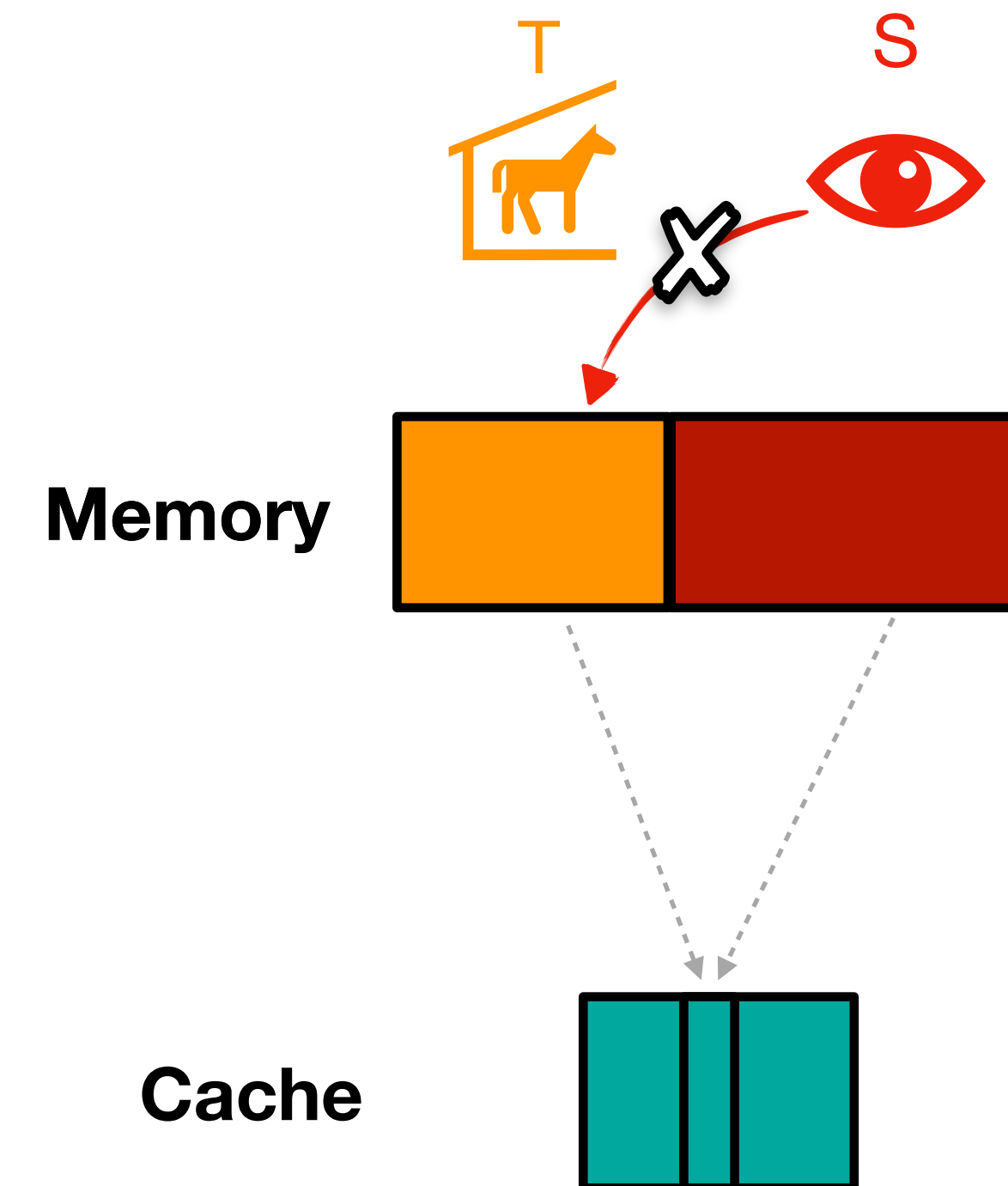
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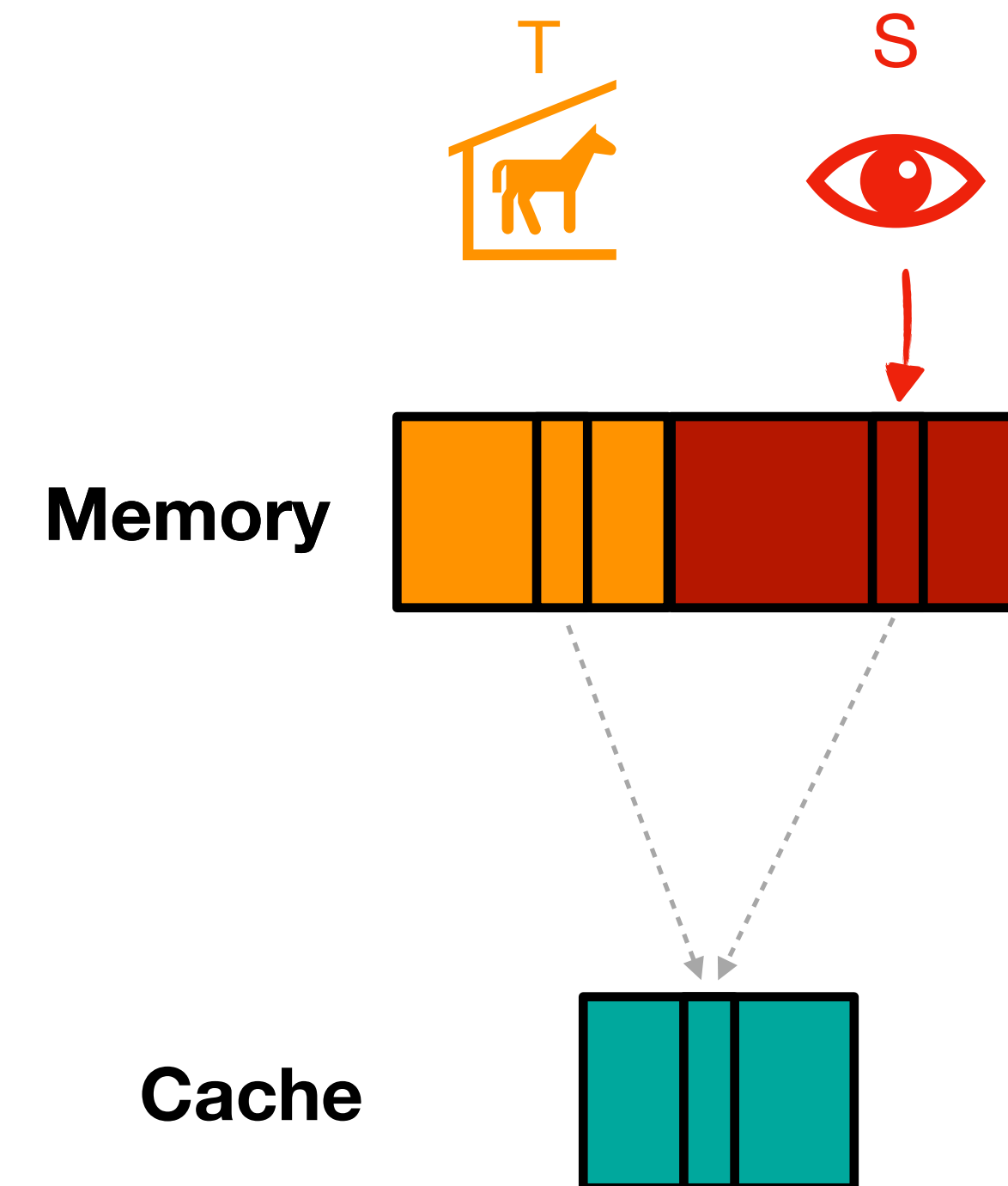
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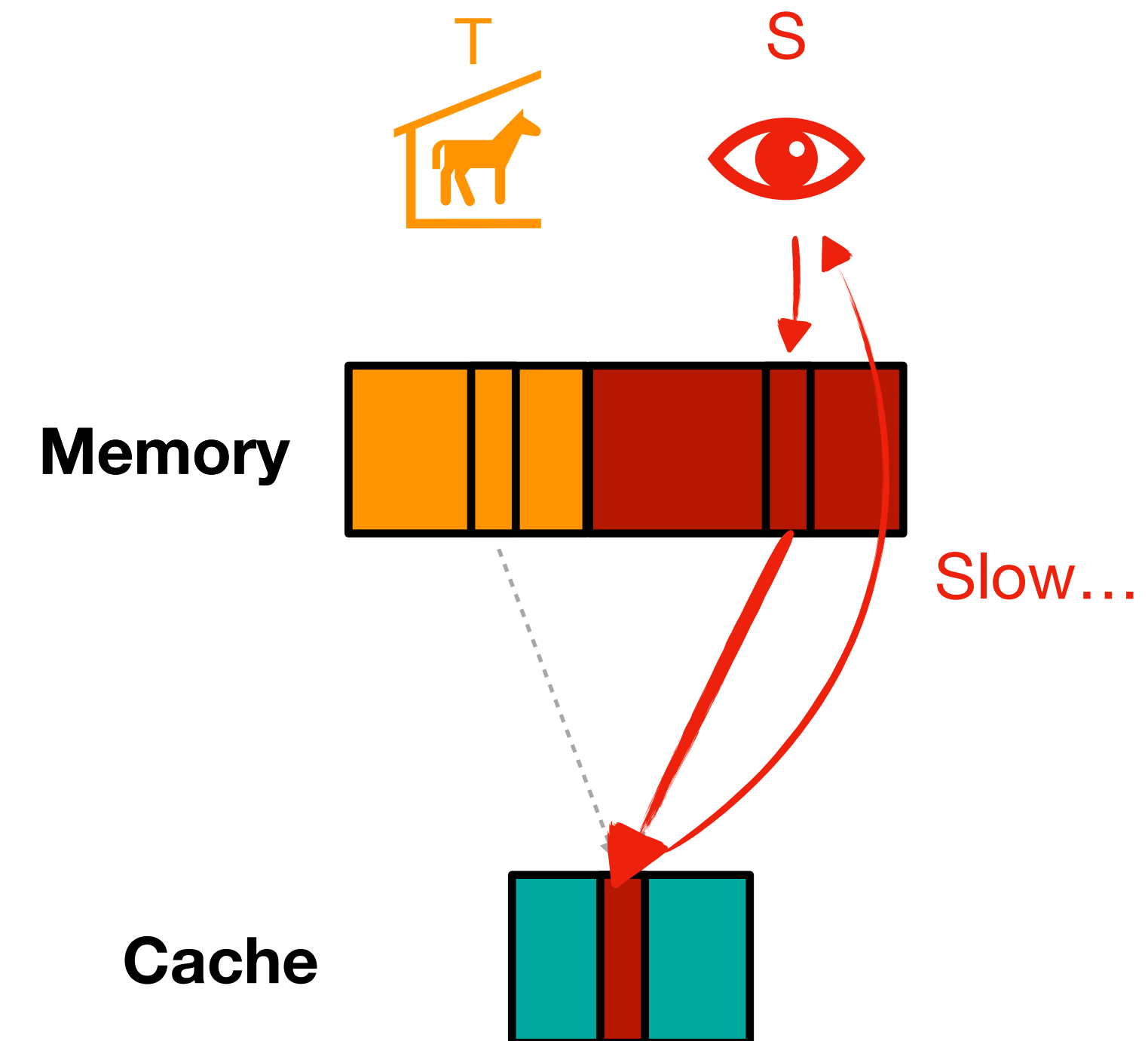
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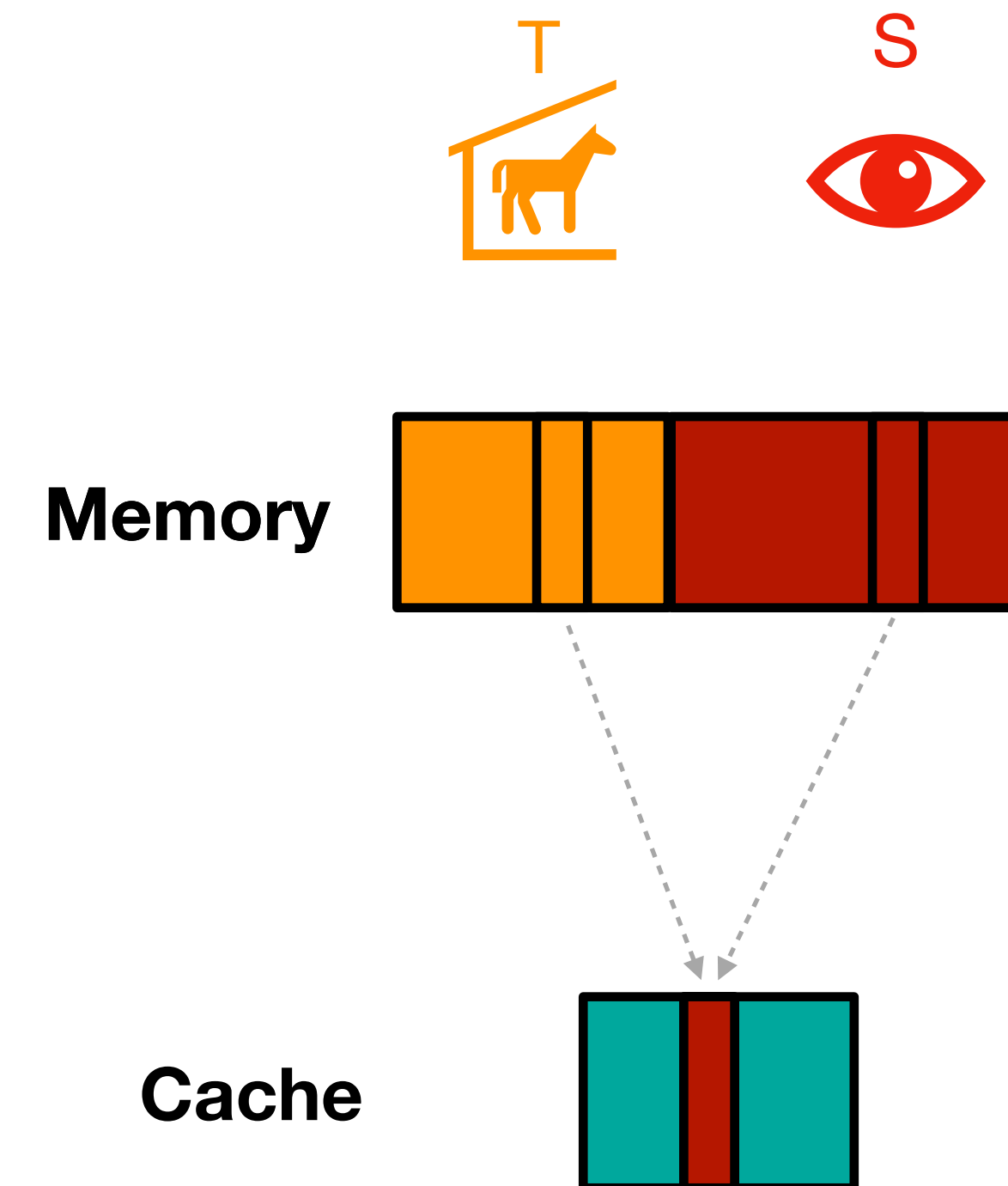
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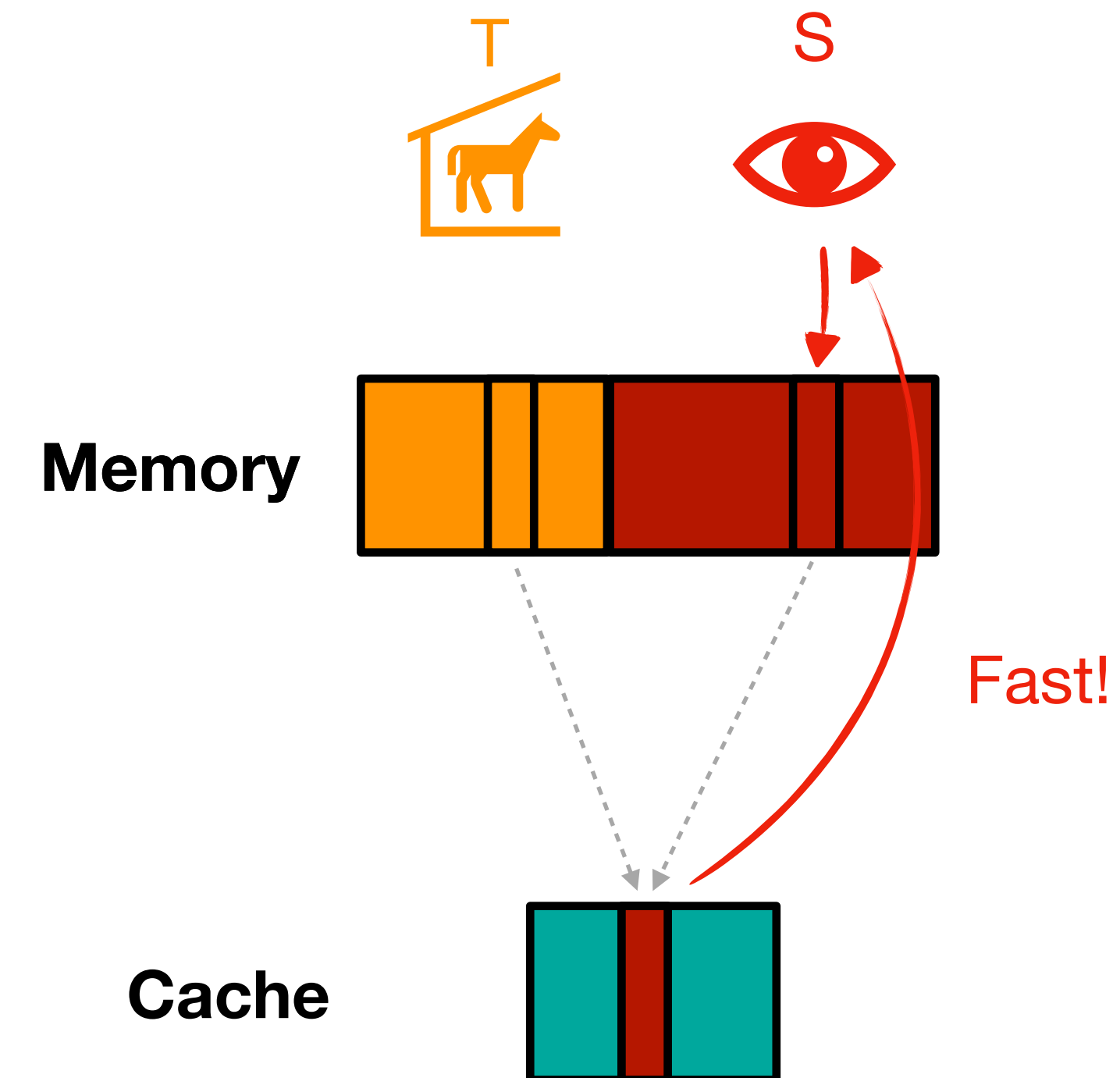
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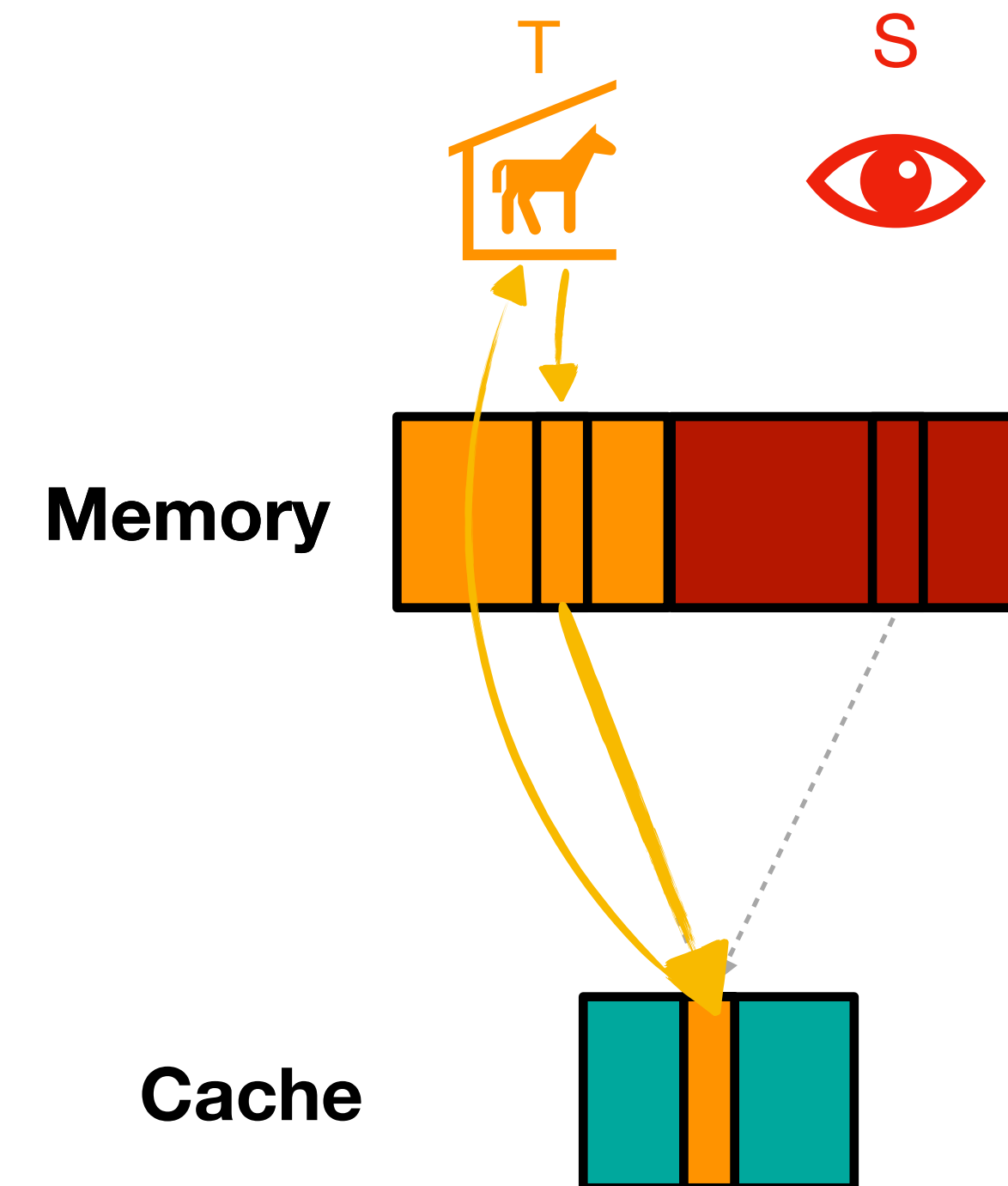
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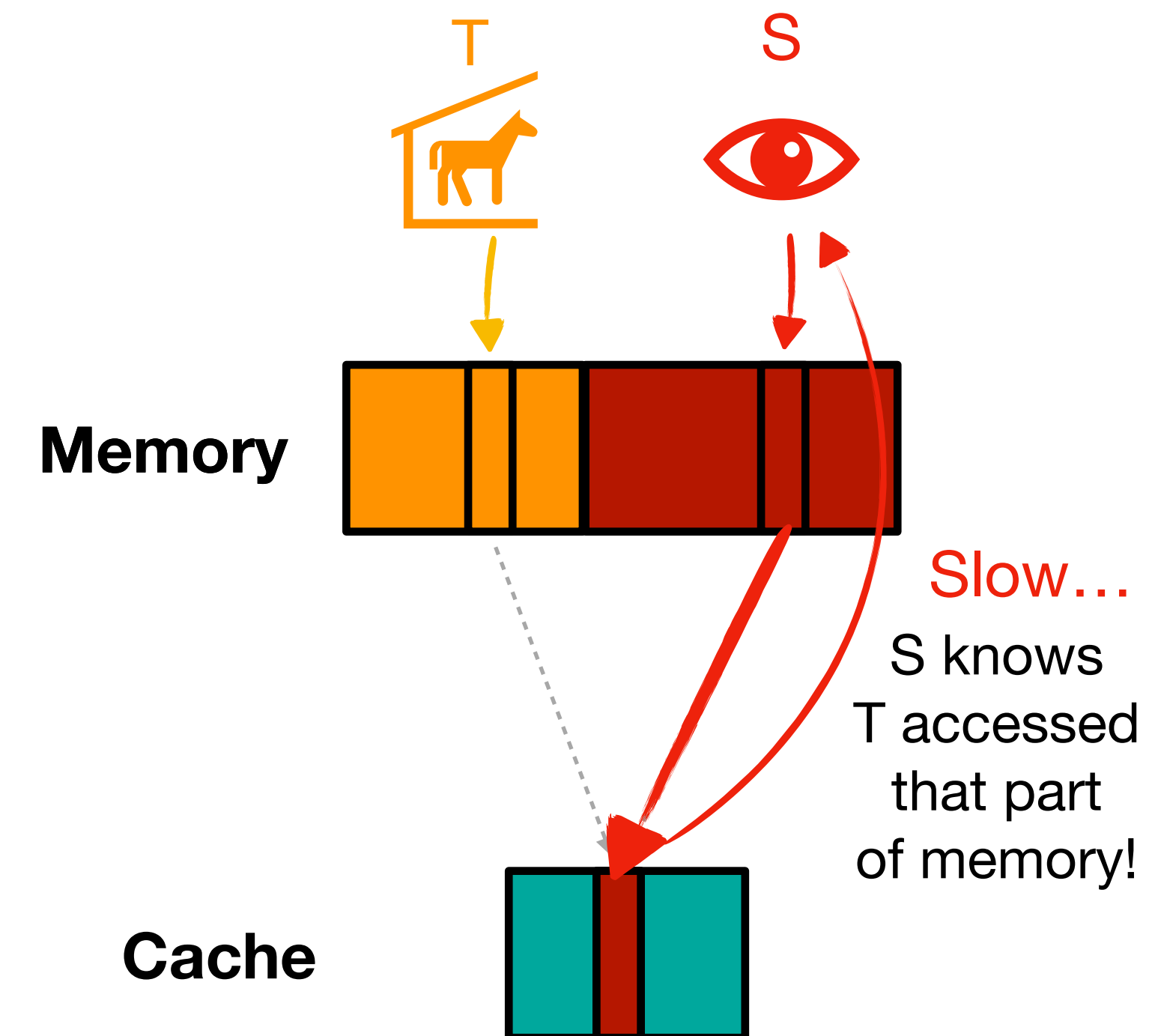
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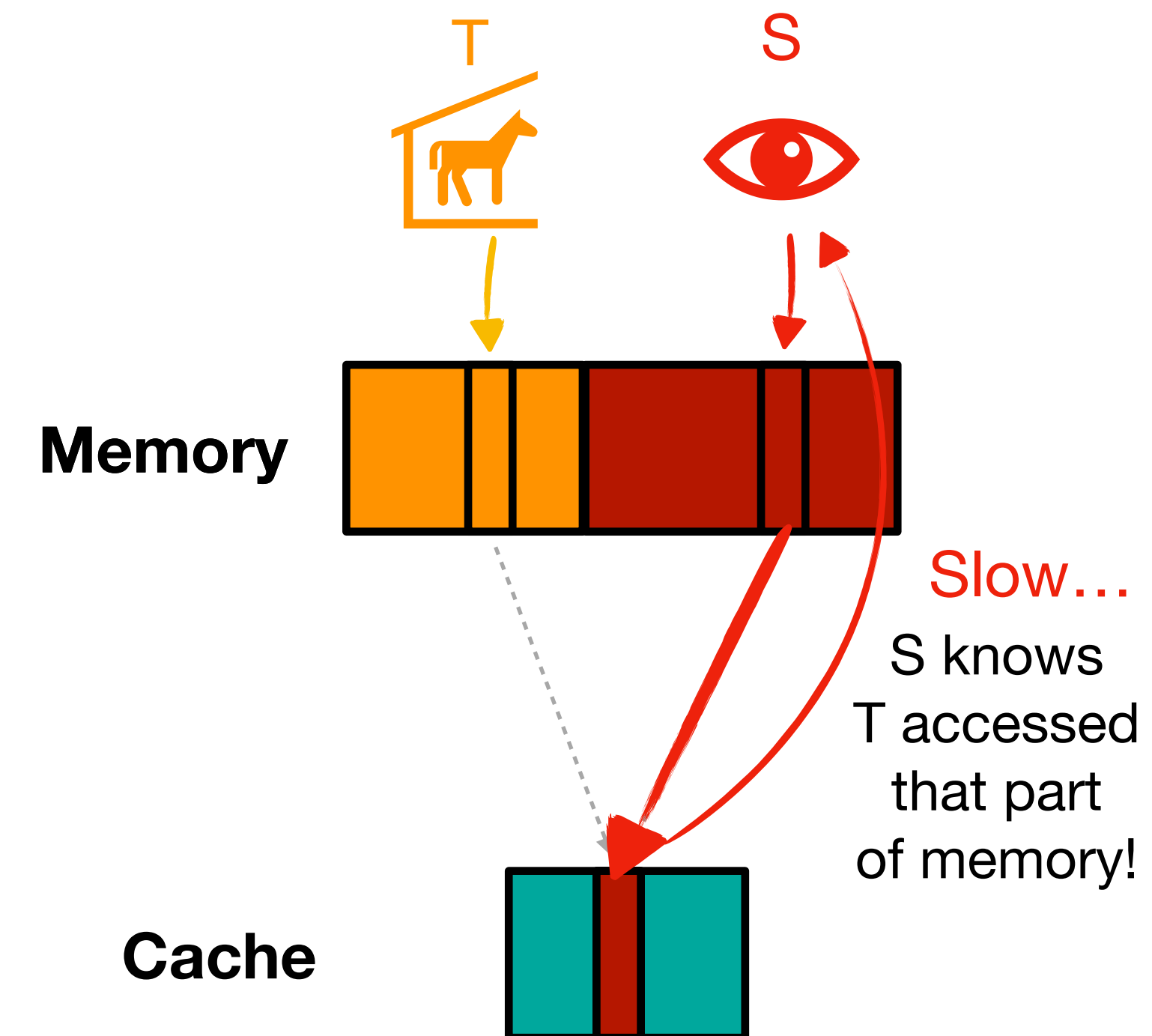


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Gernot Heiser

with
Yuval Yarom (U. Adelaide)
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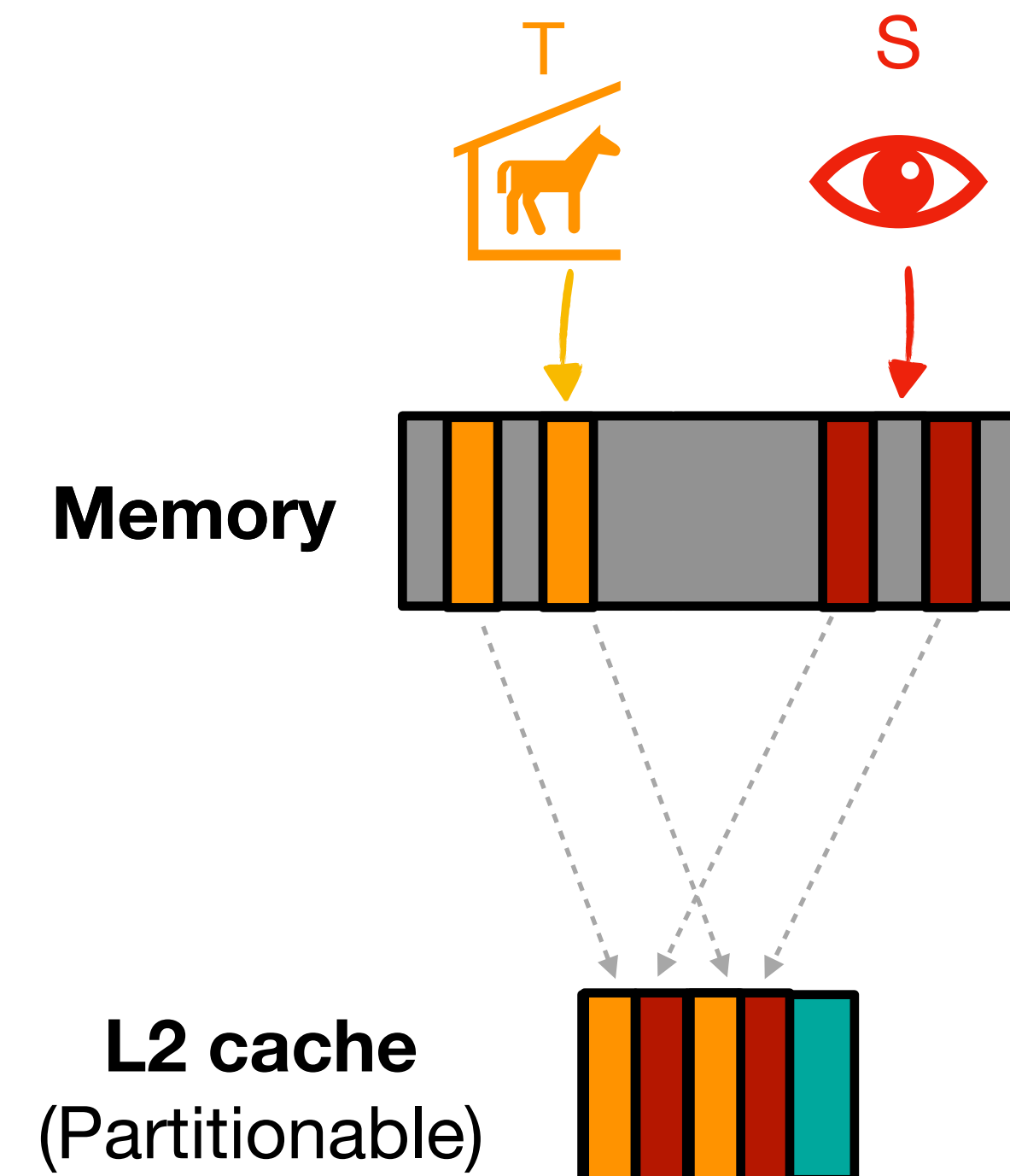


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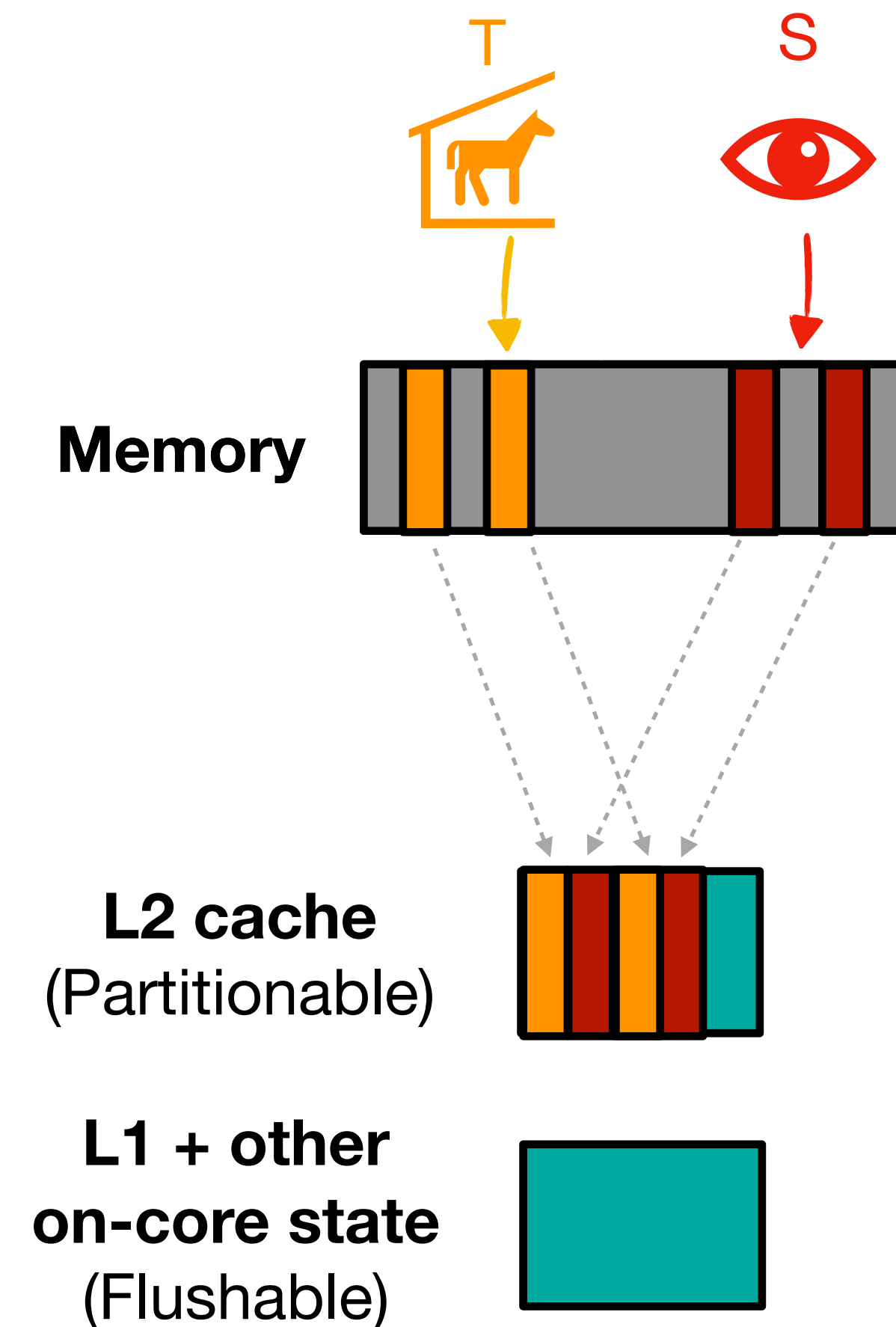


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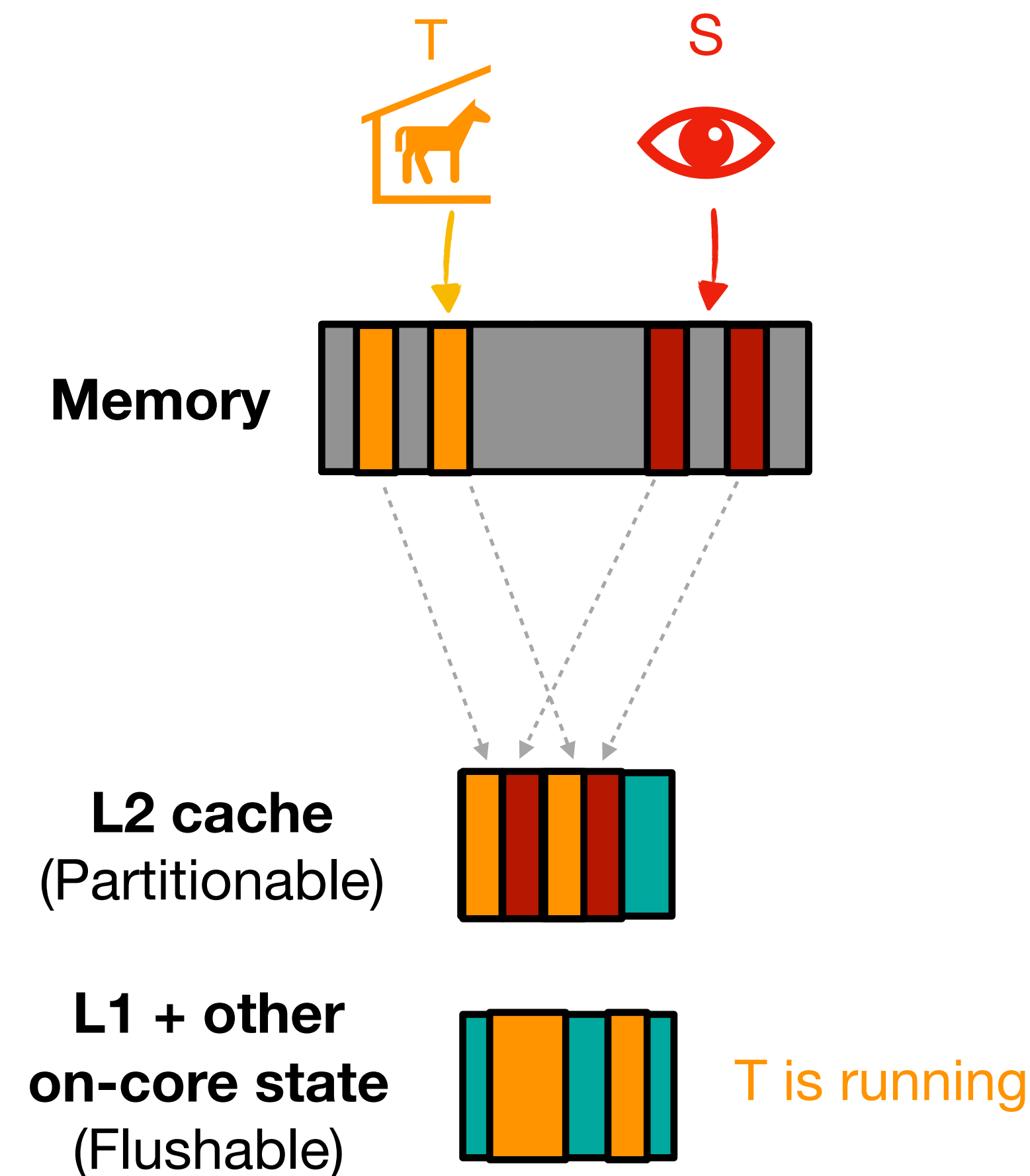


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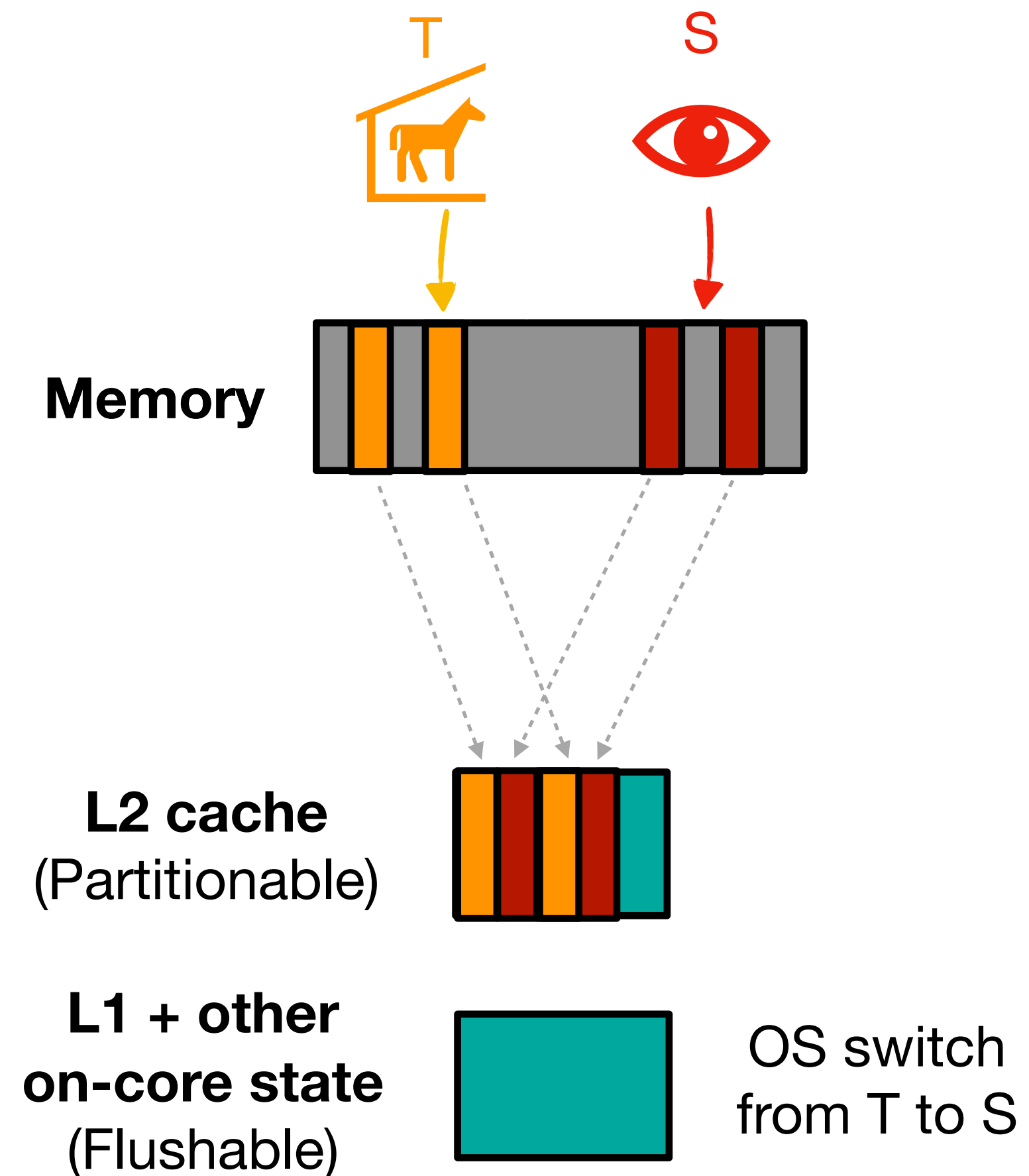


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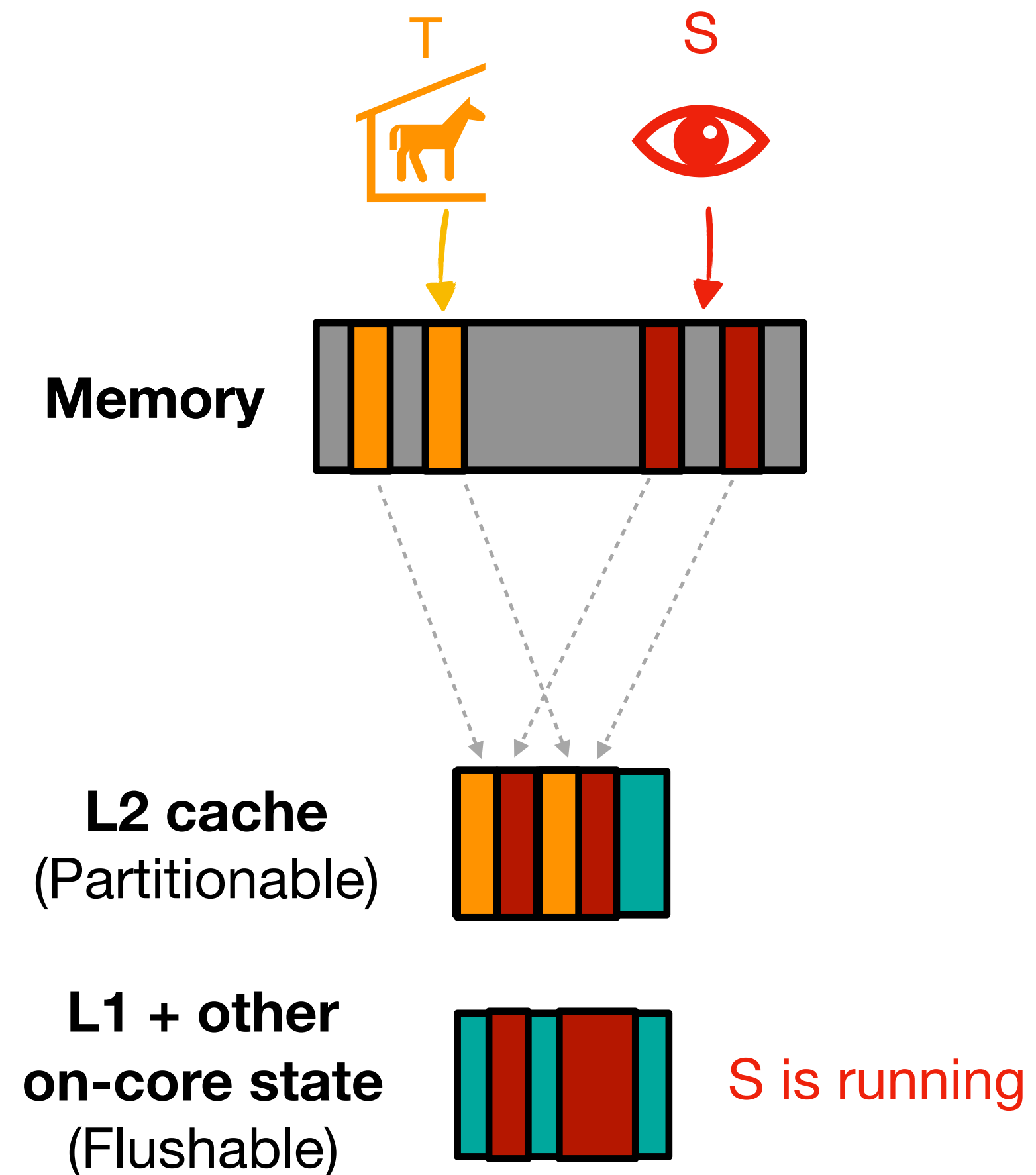


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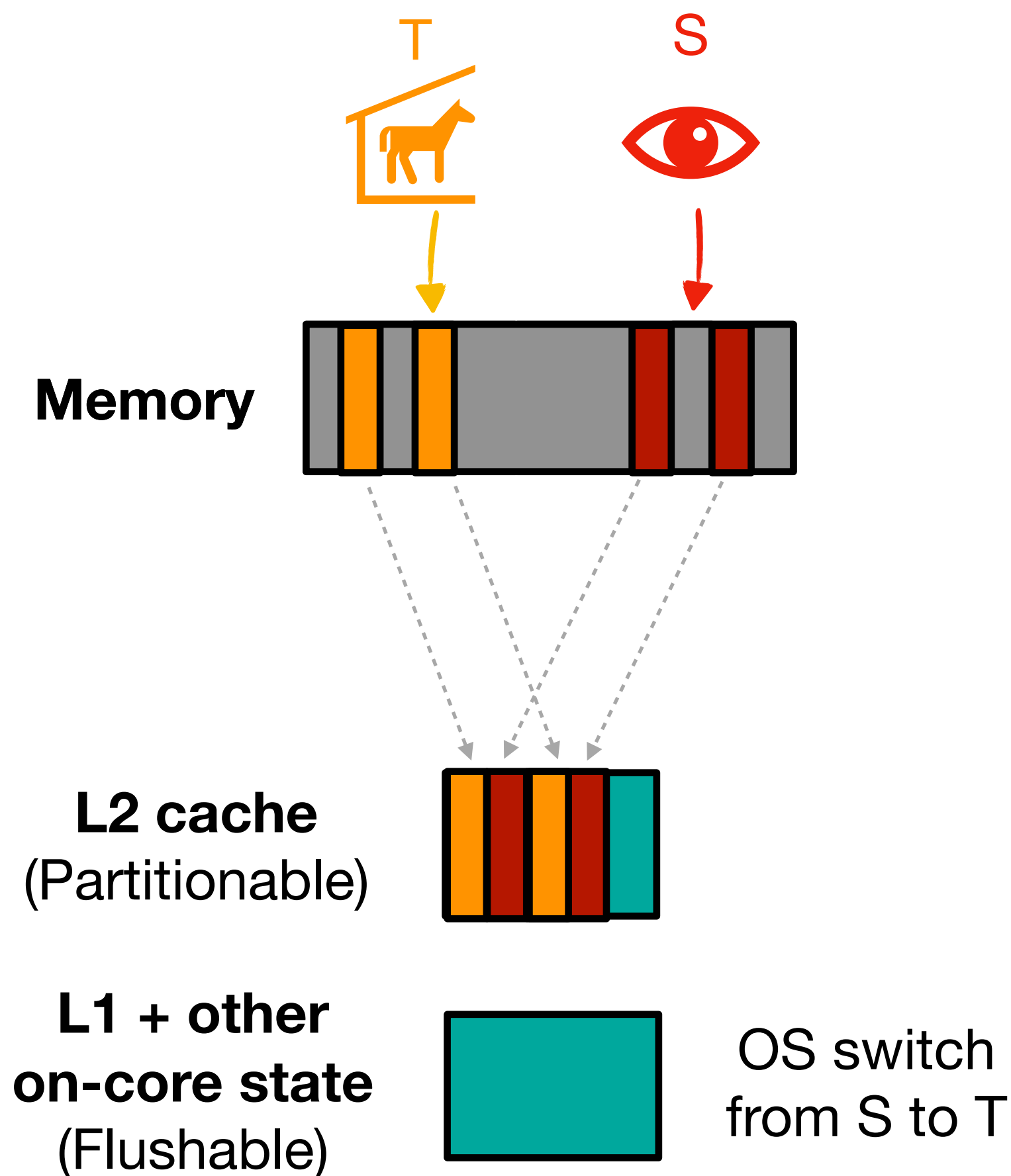


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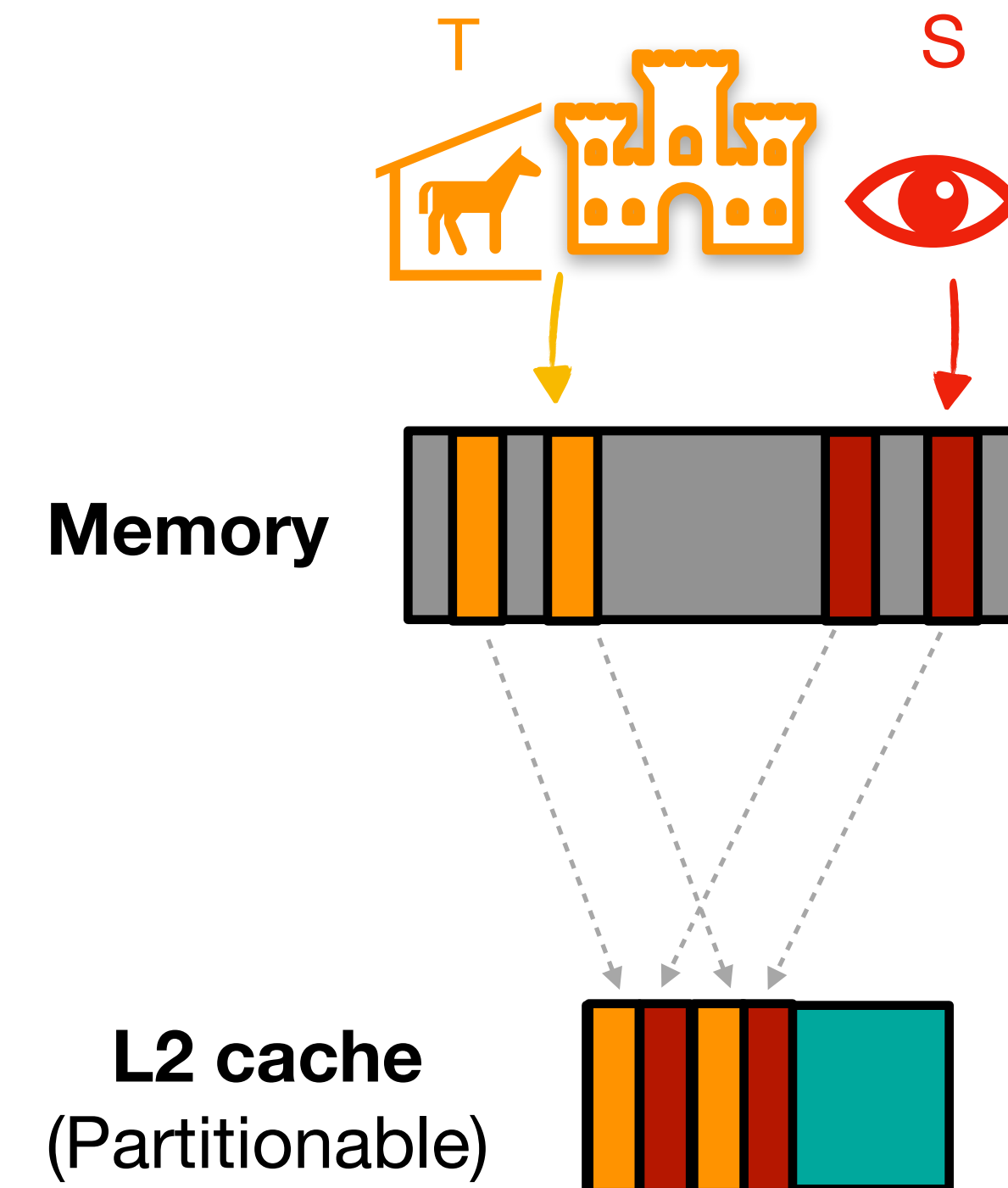


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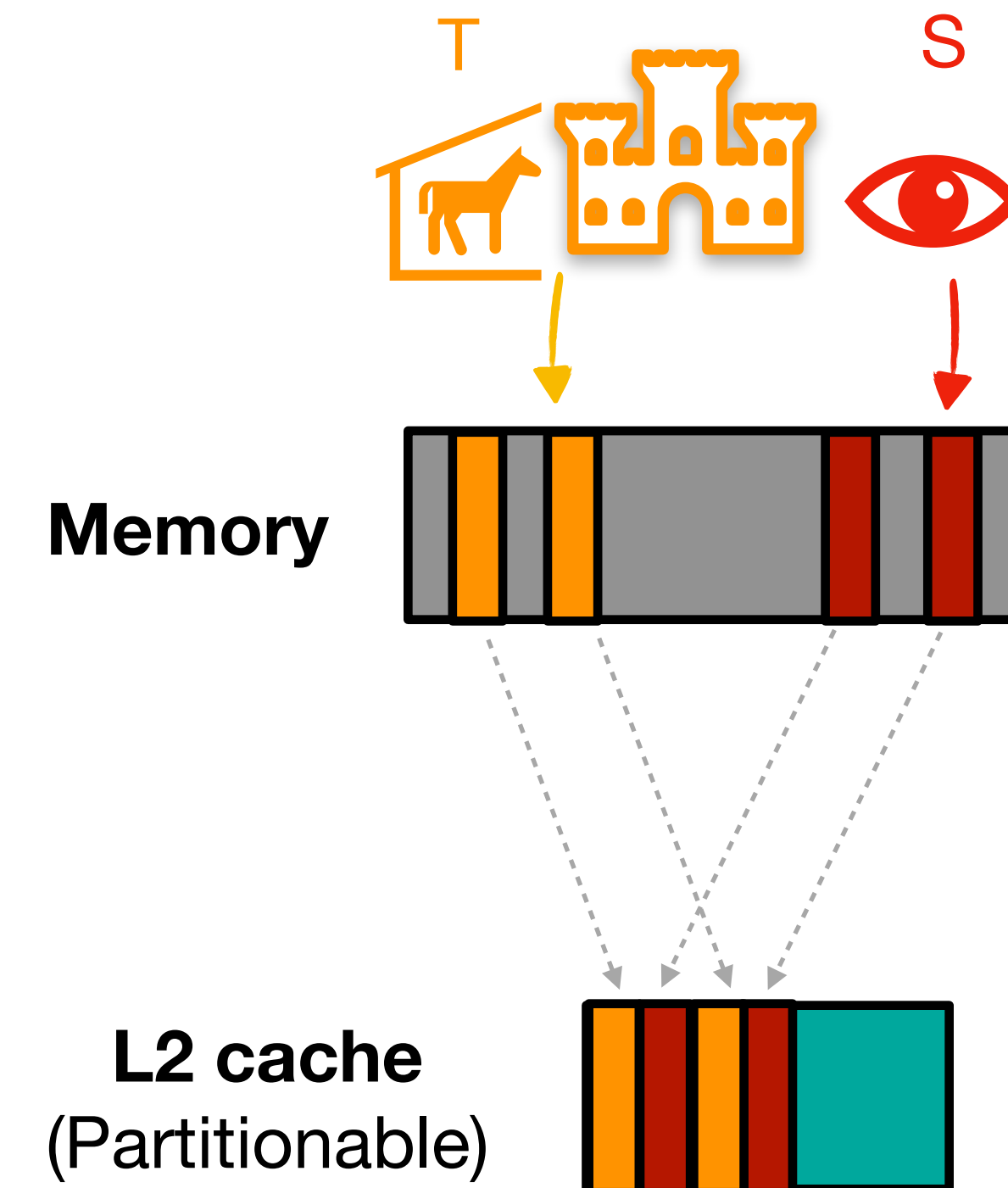
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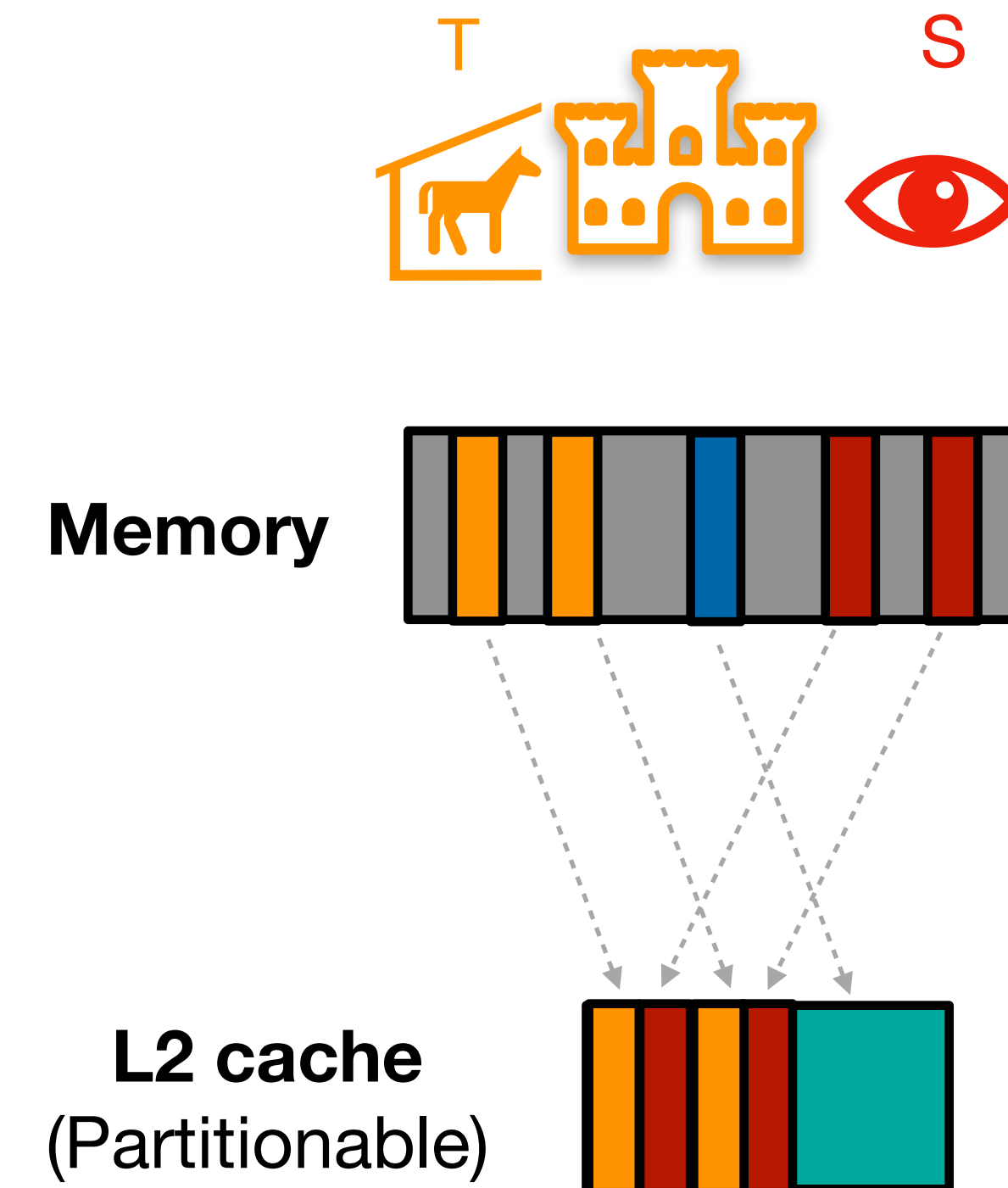
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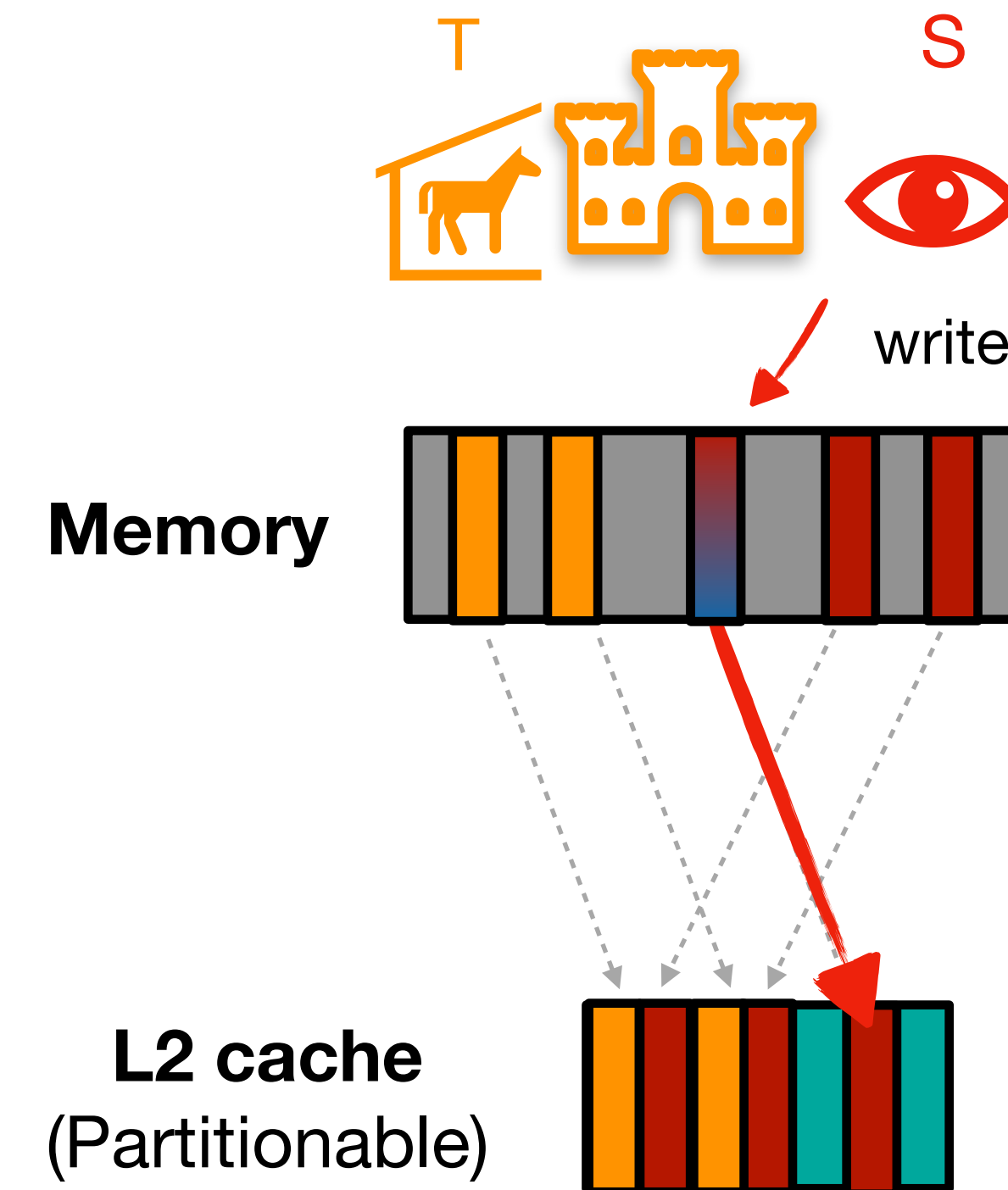
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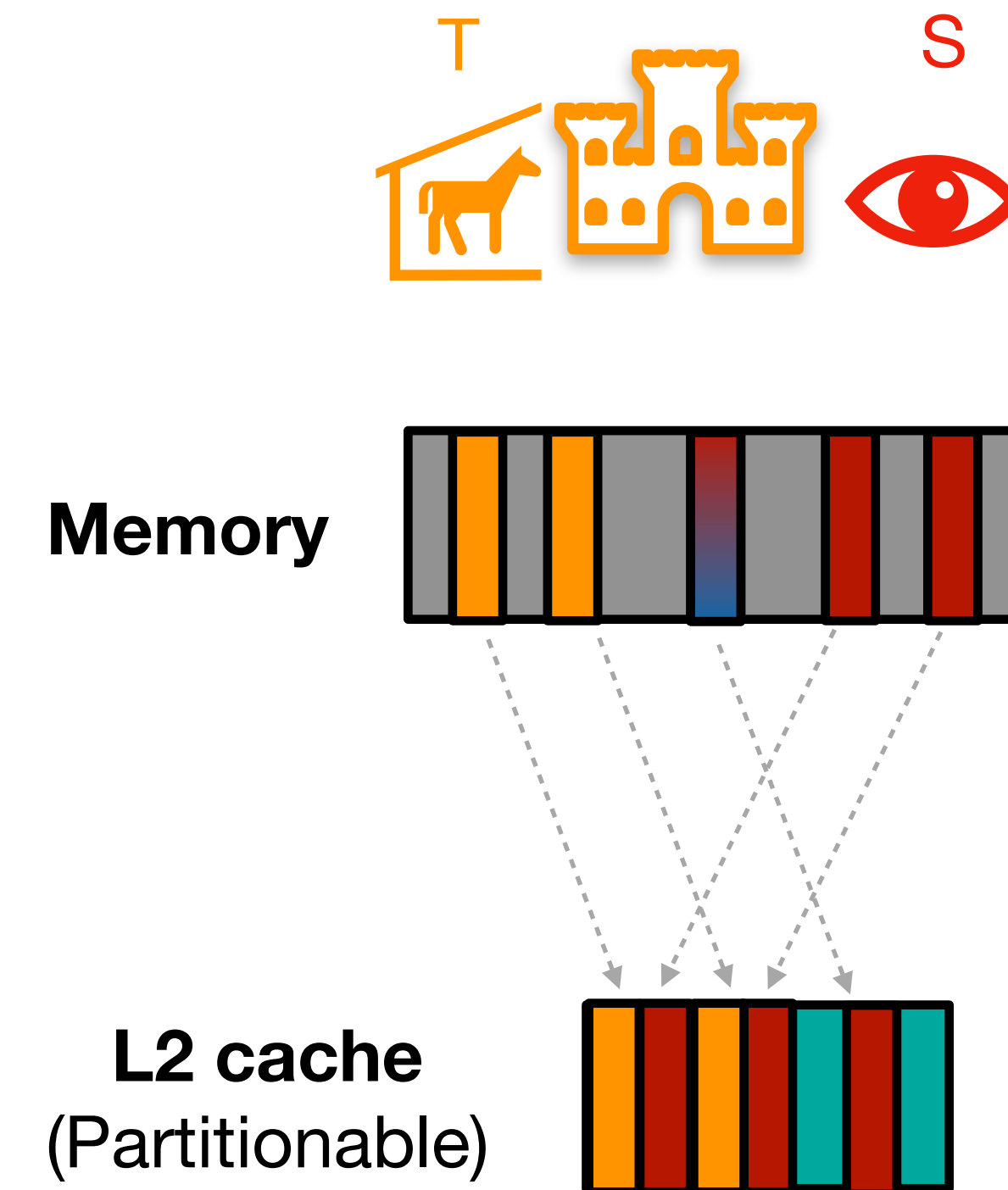
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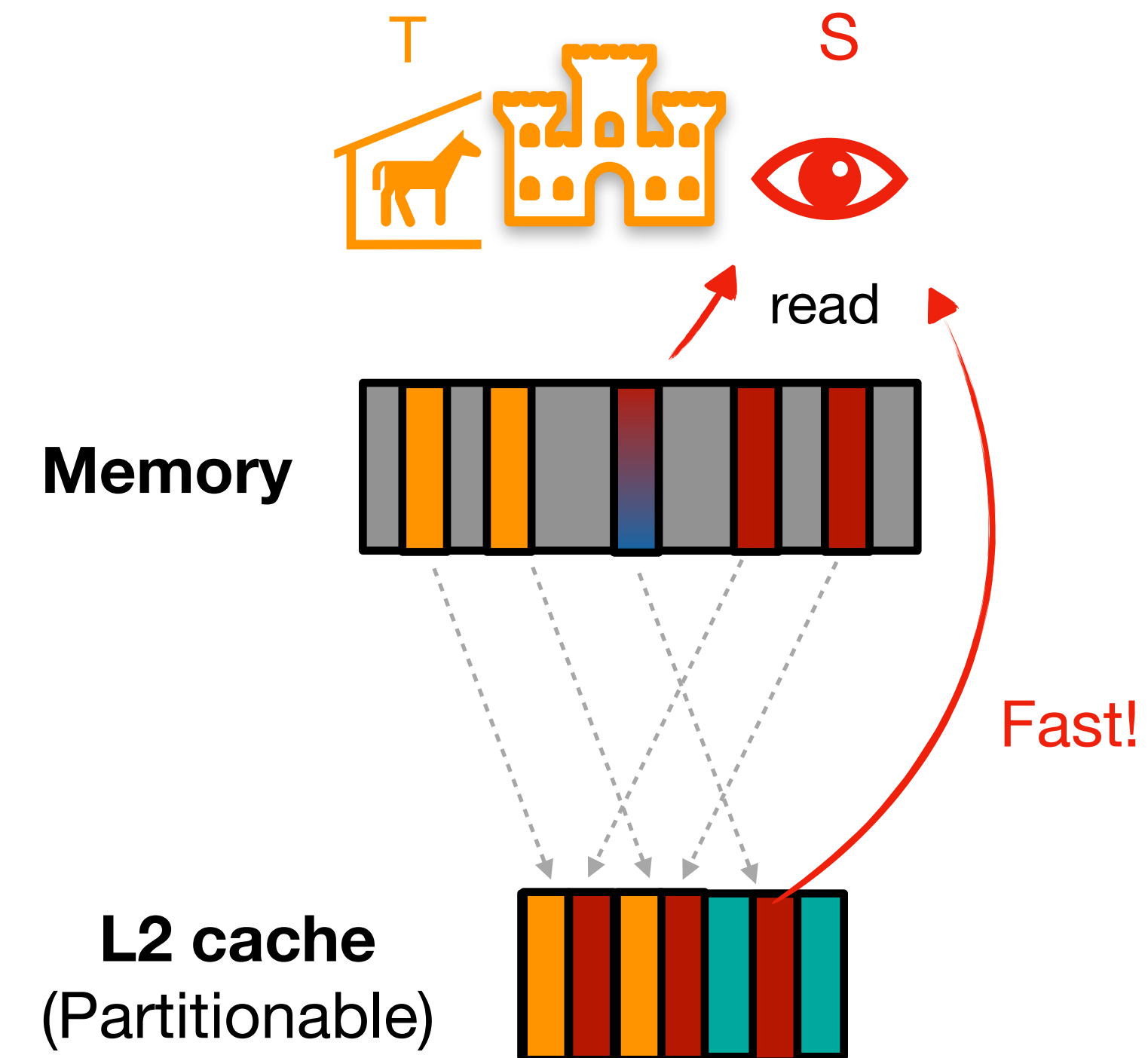
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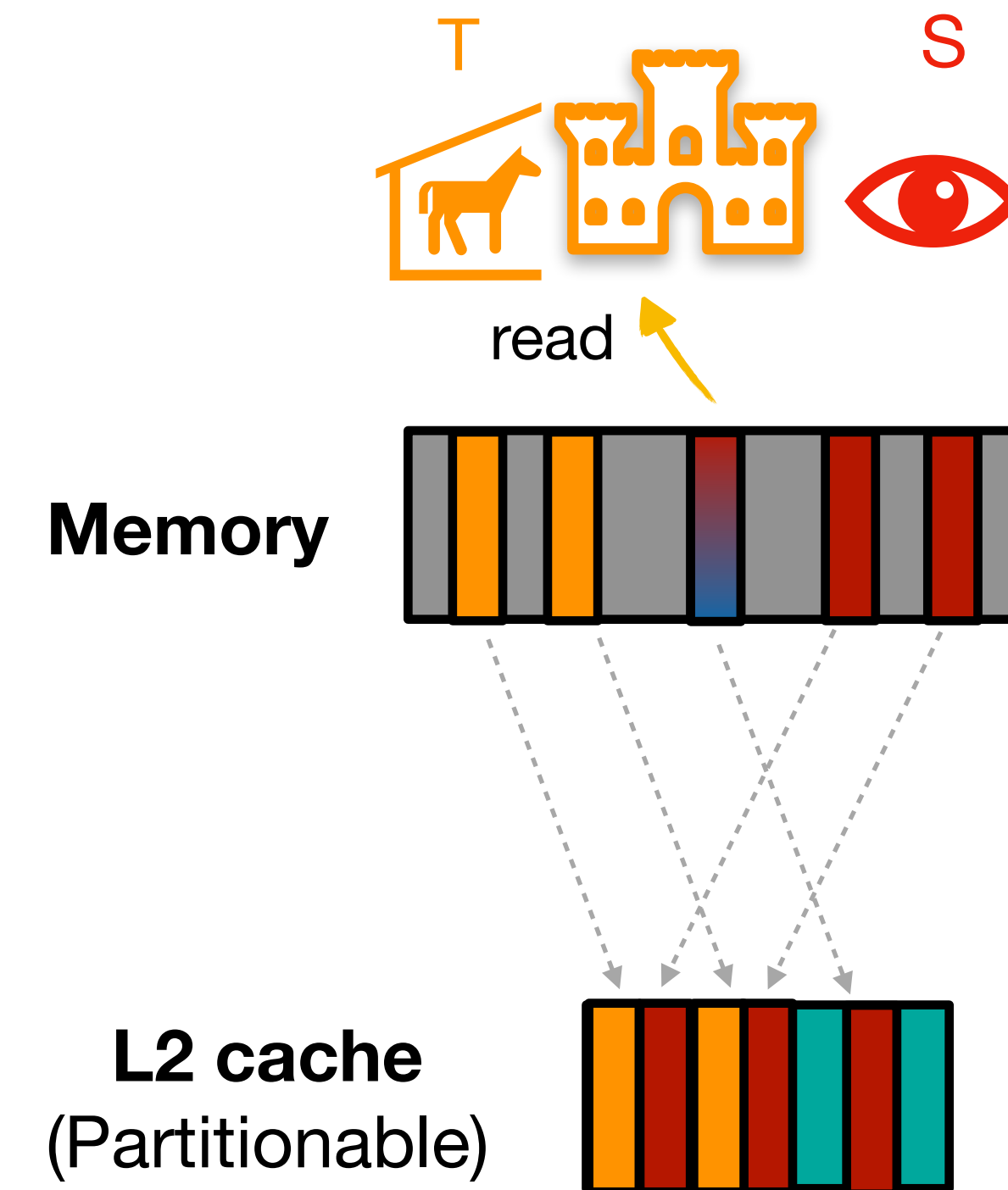
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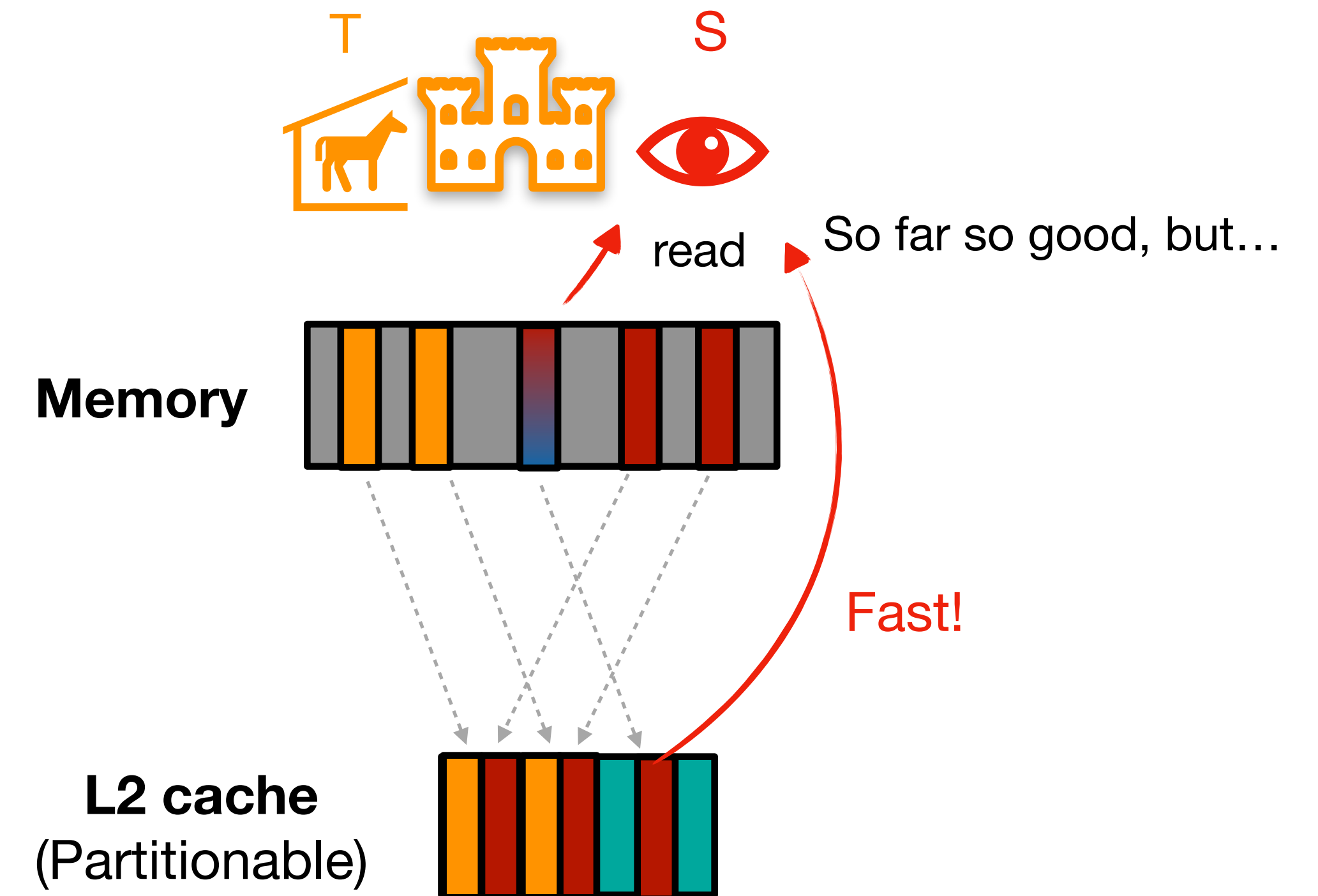
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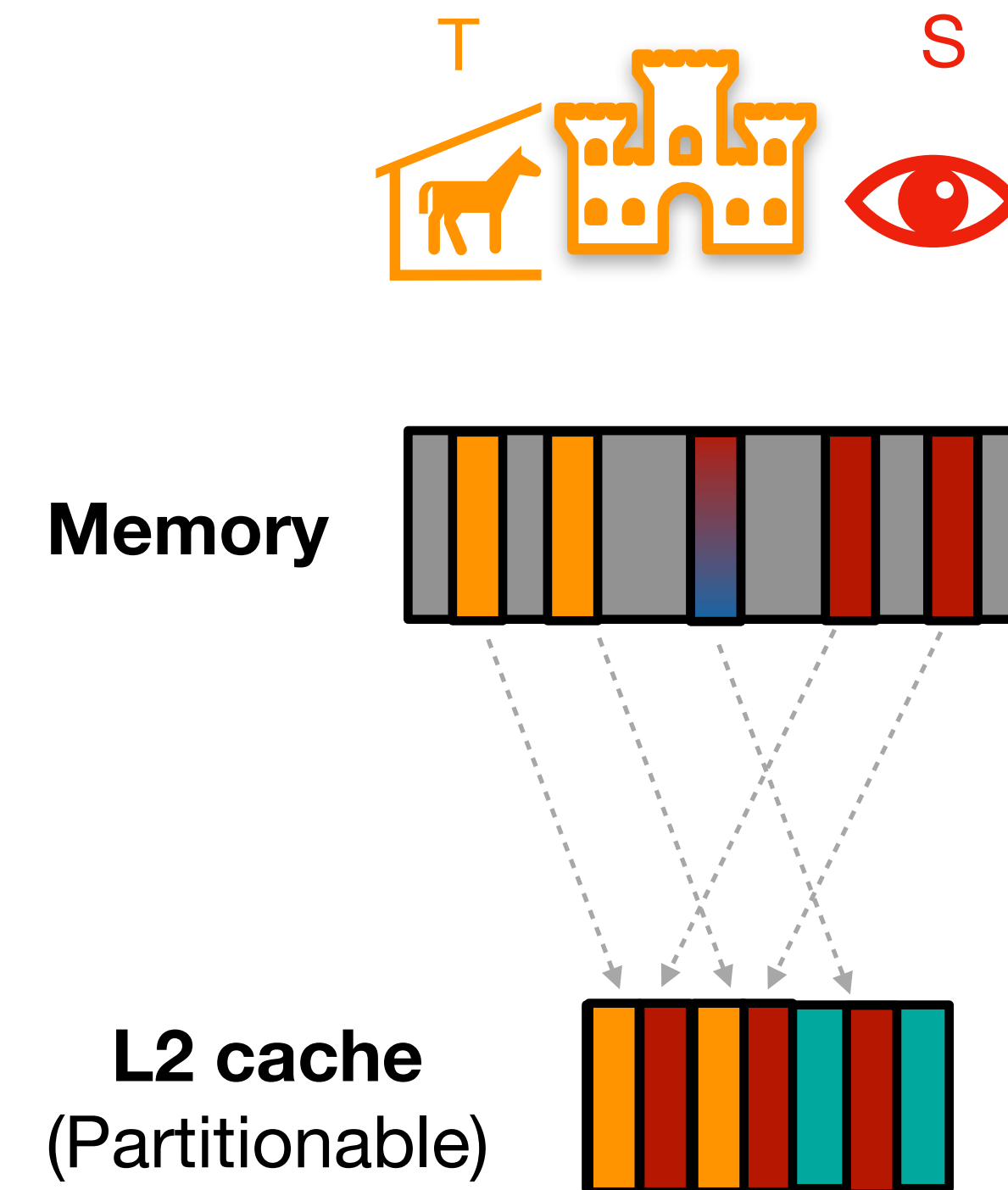


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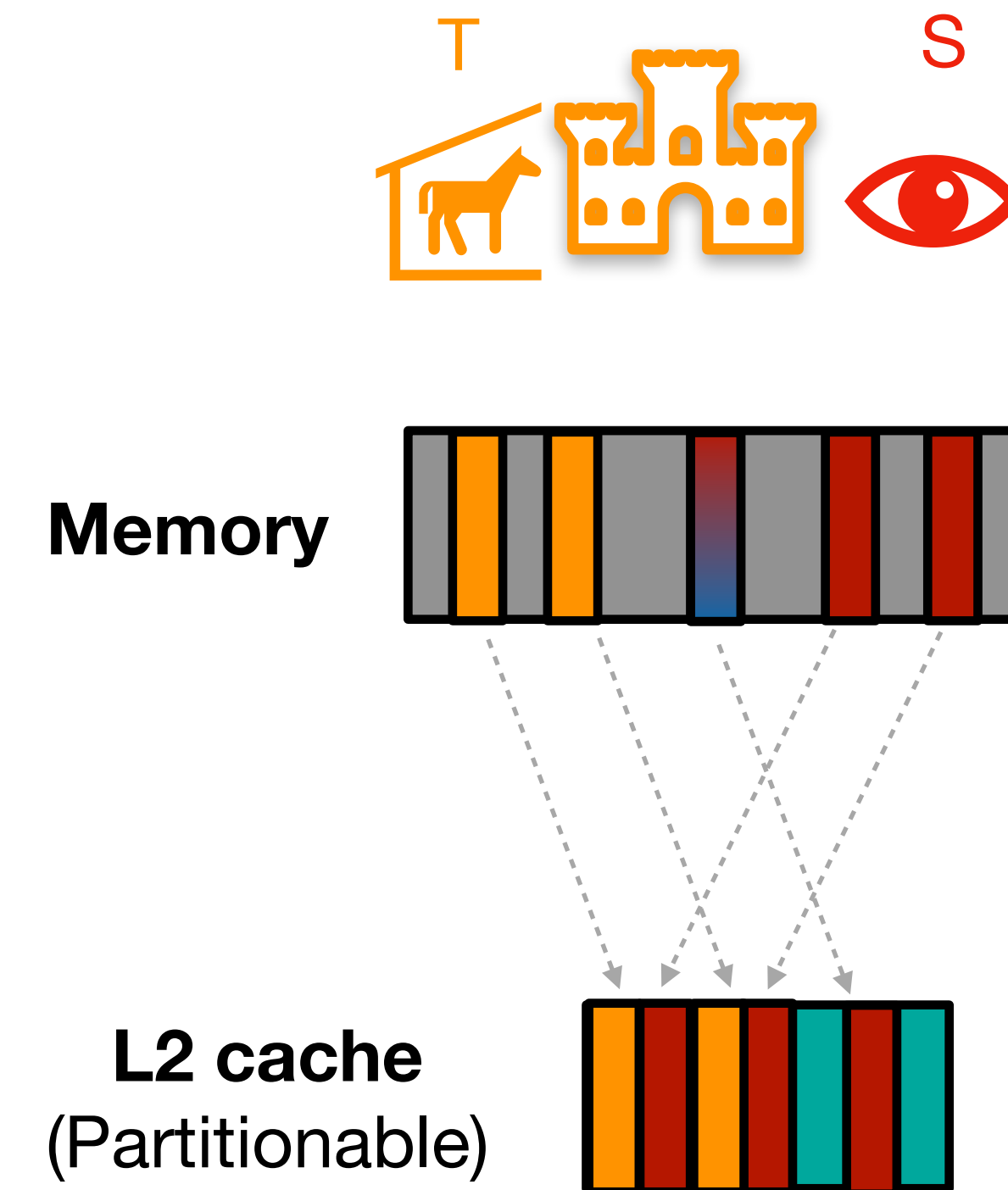


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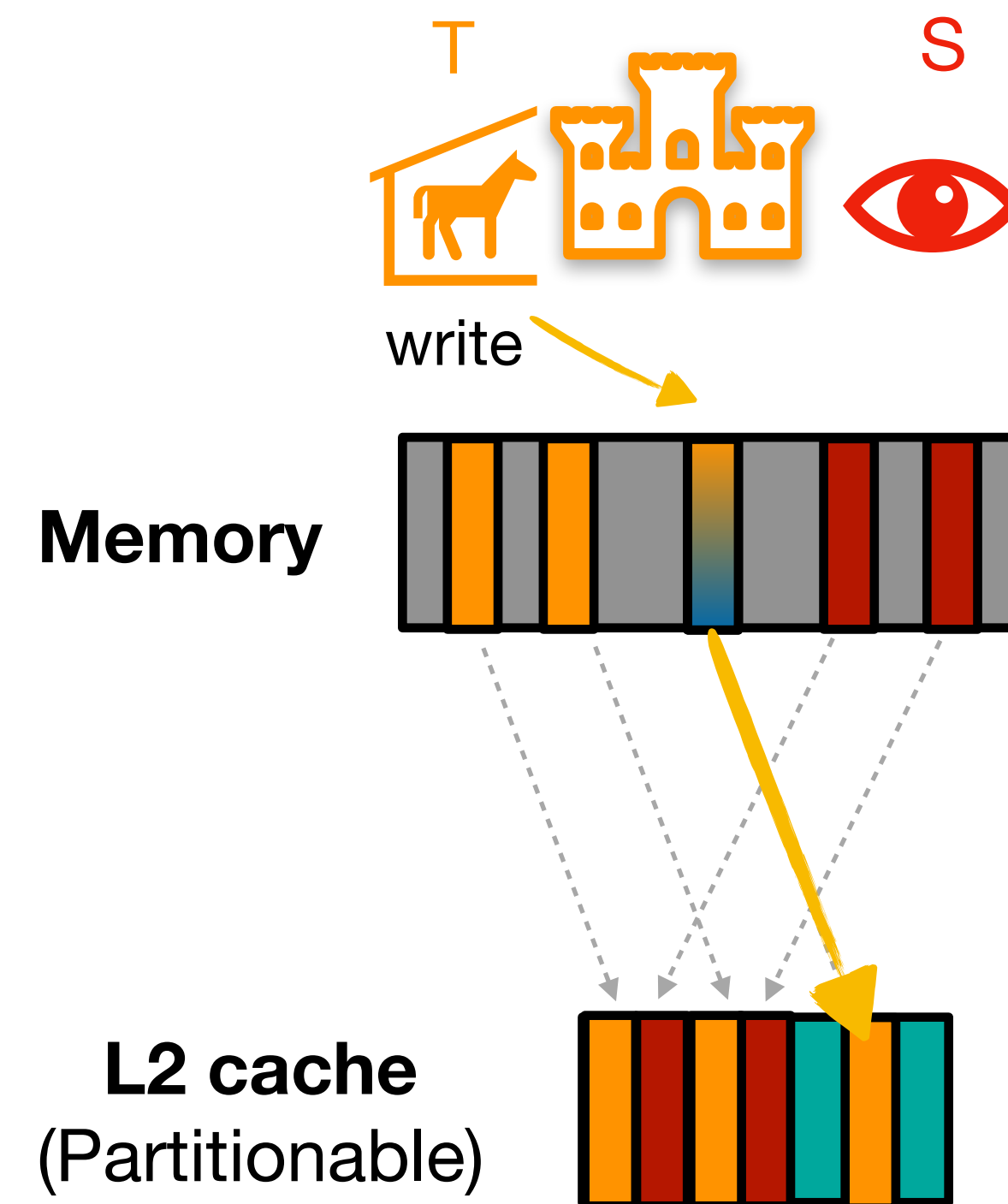


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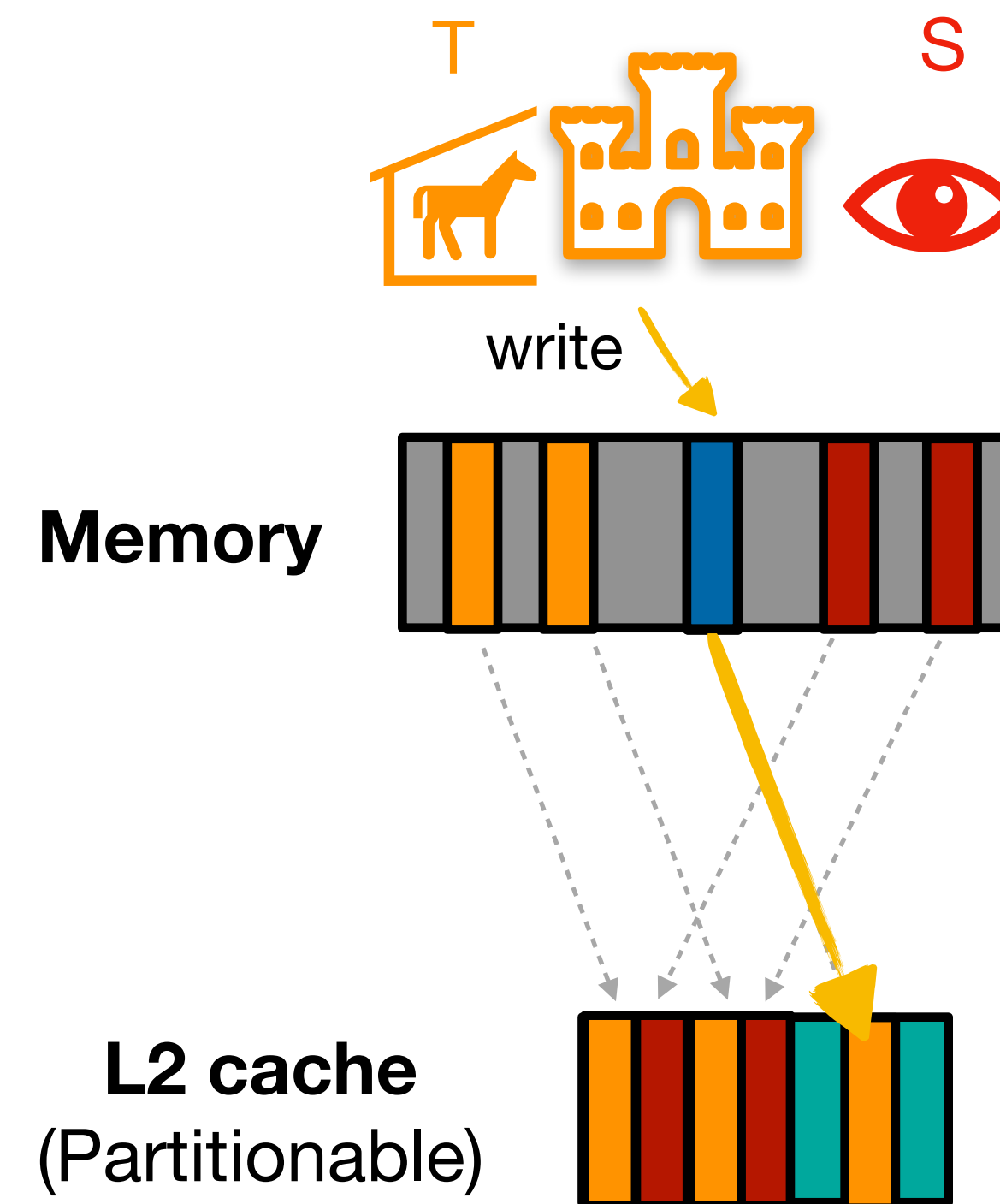


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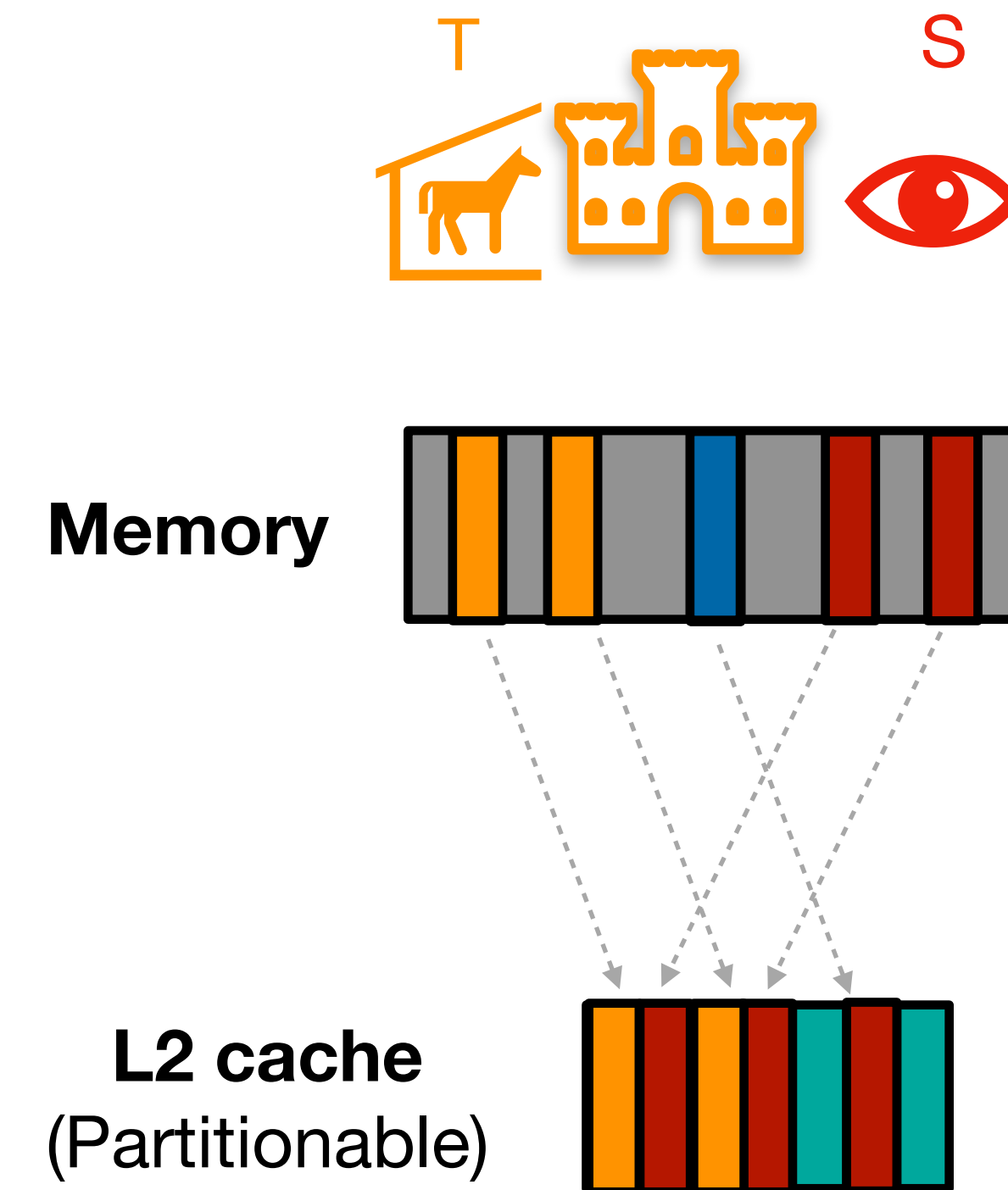


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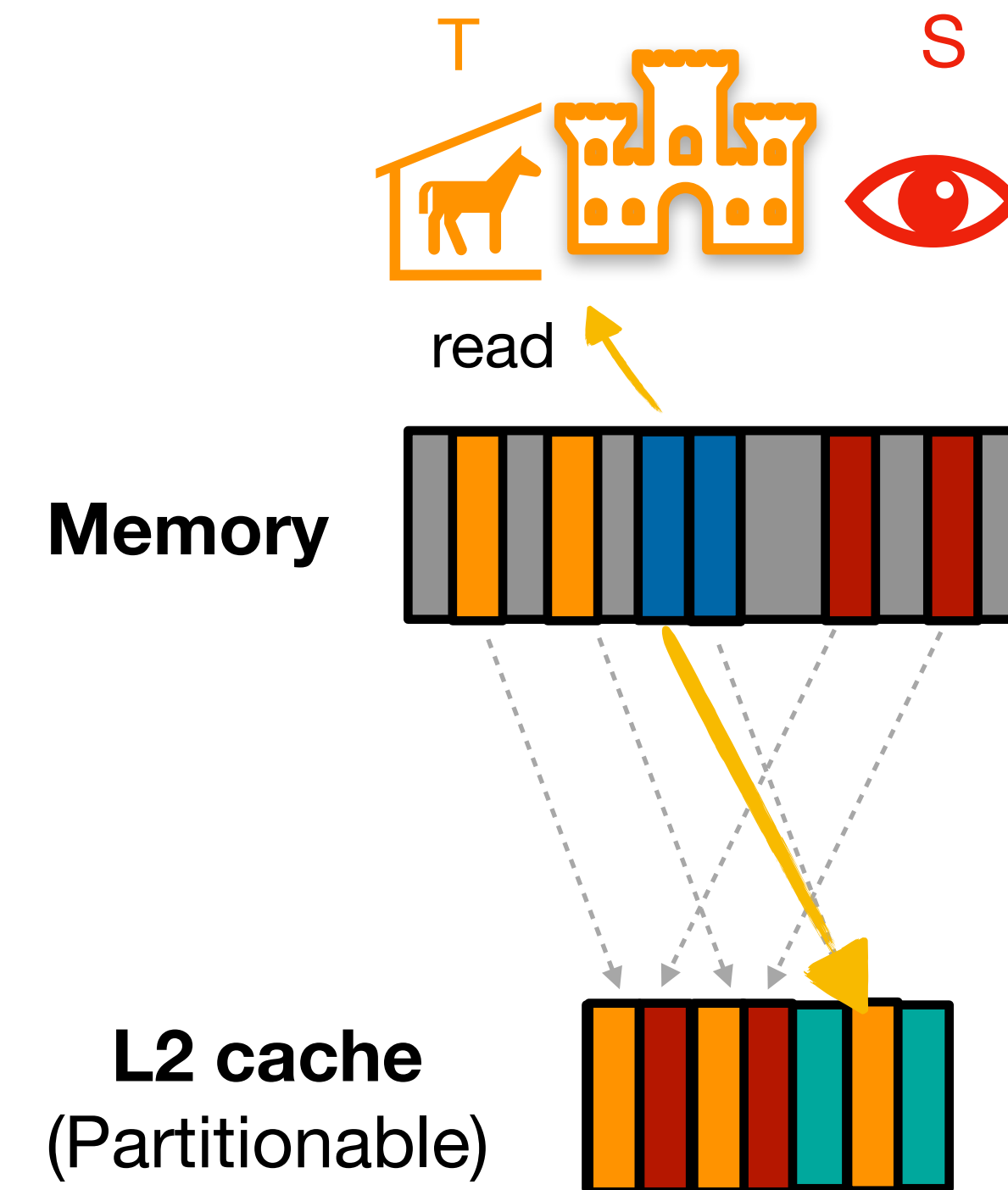


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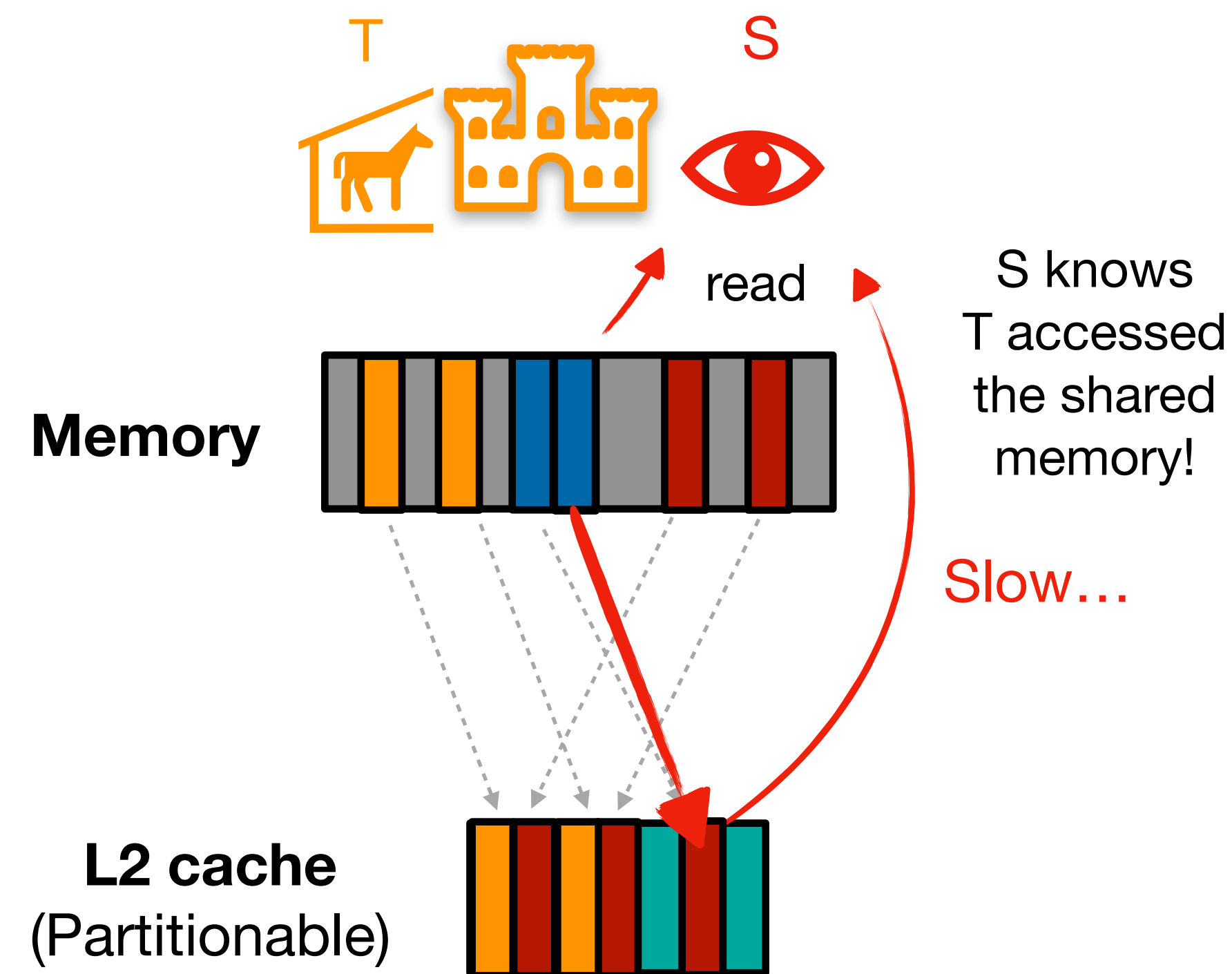


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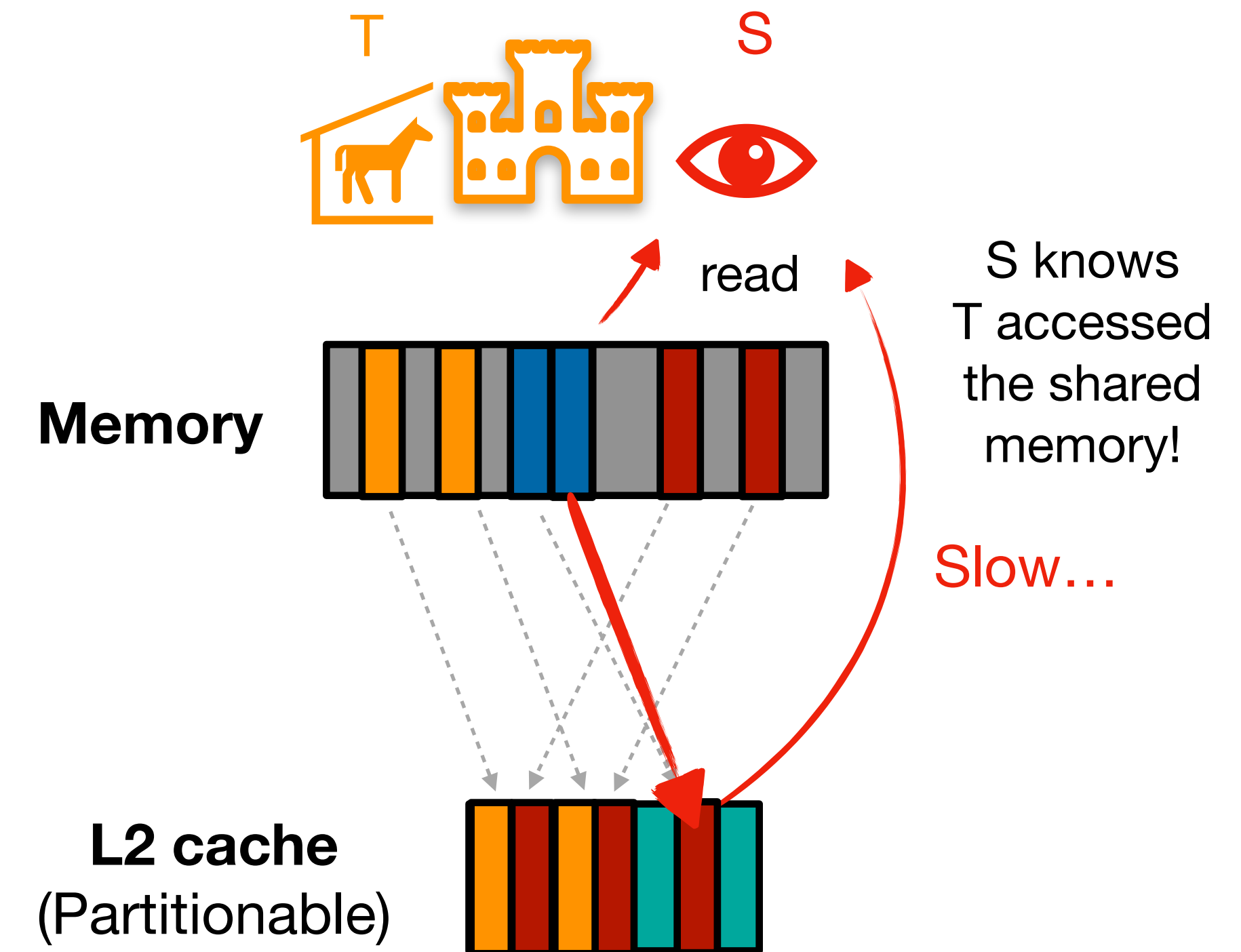
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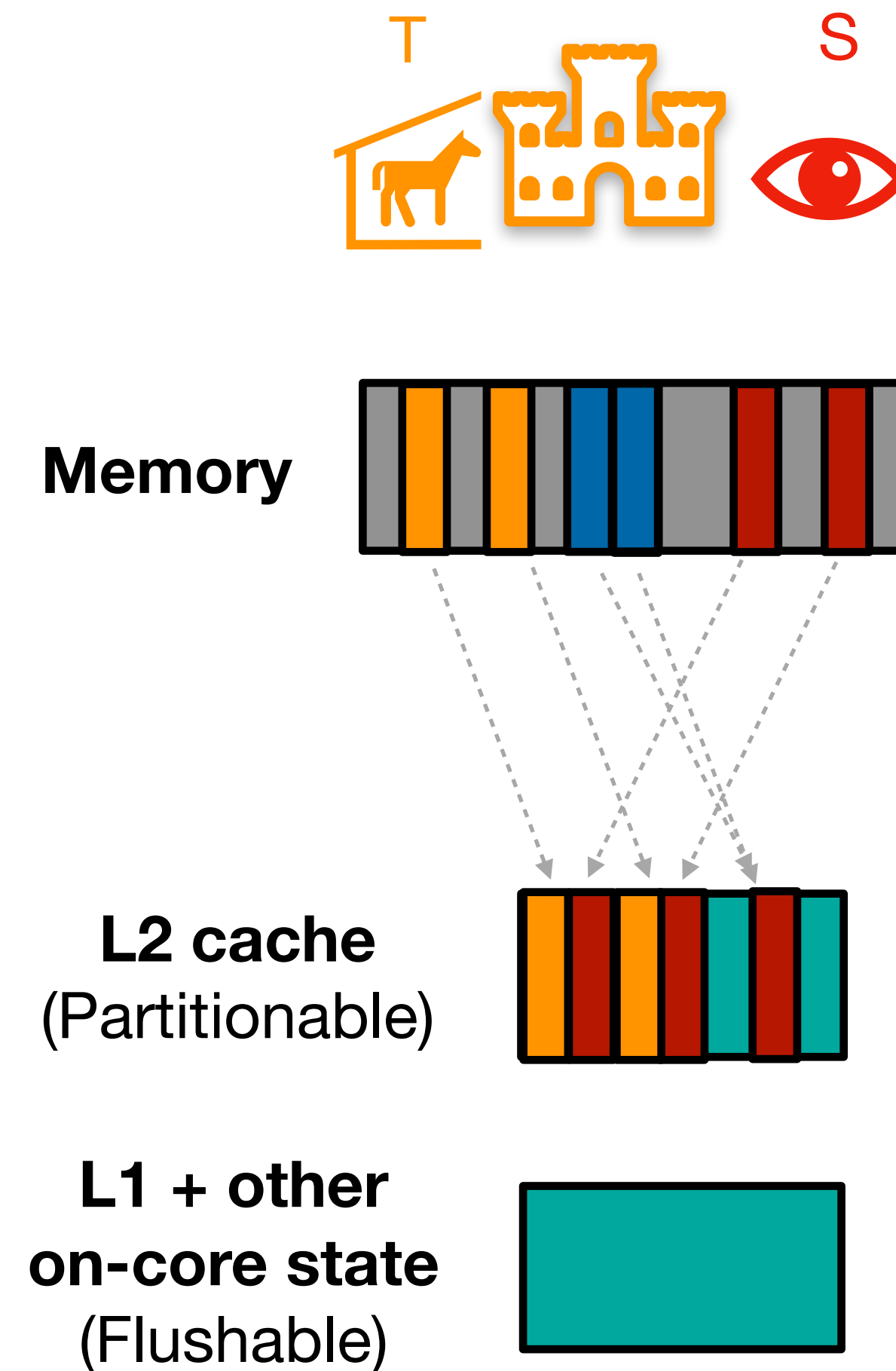
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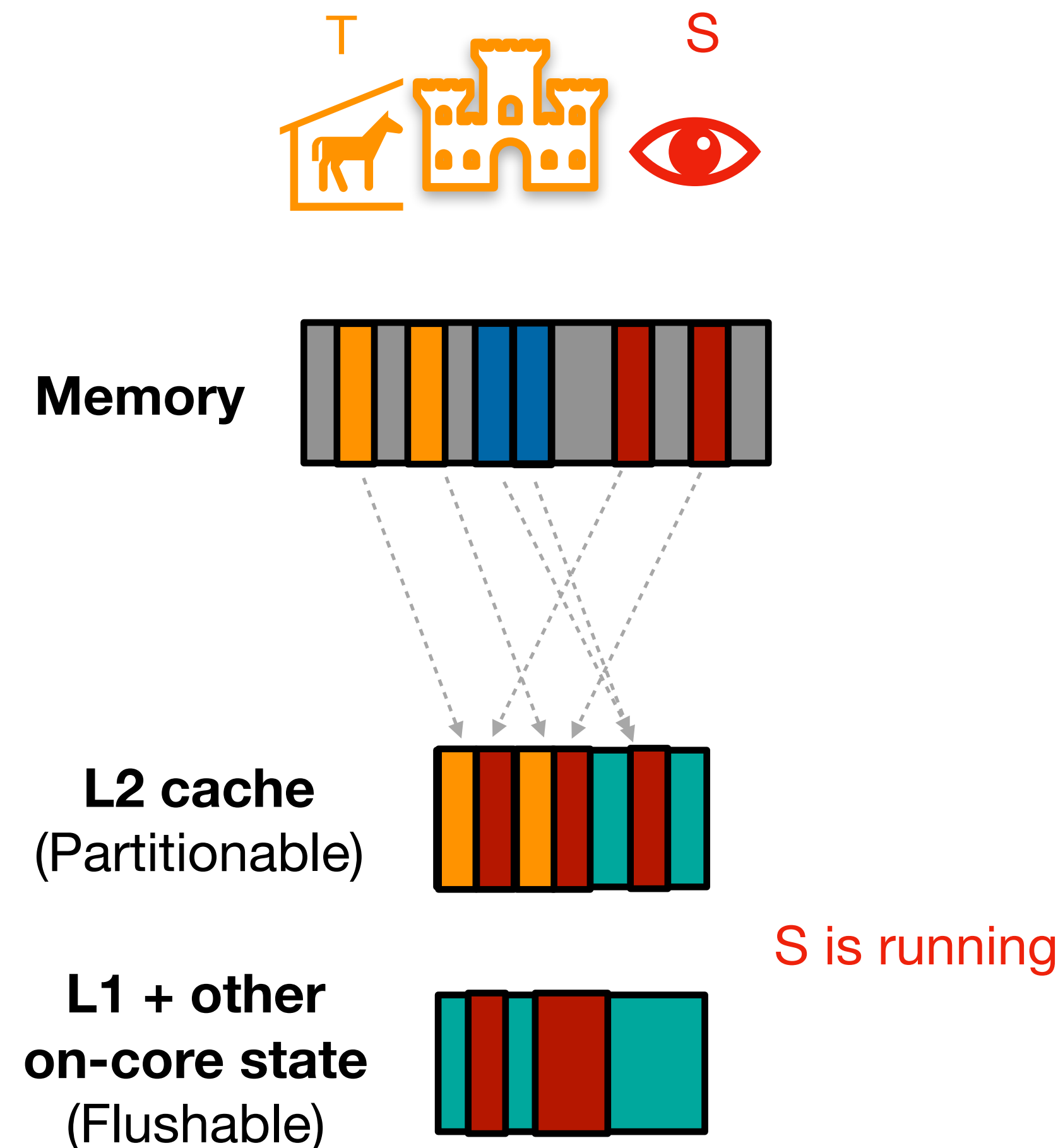
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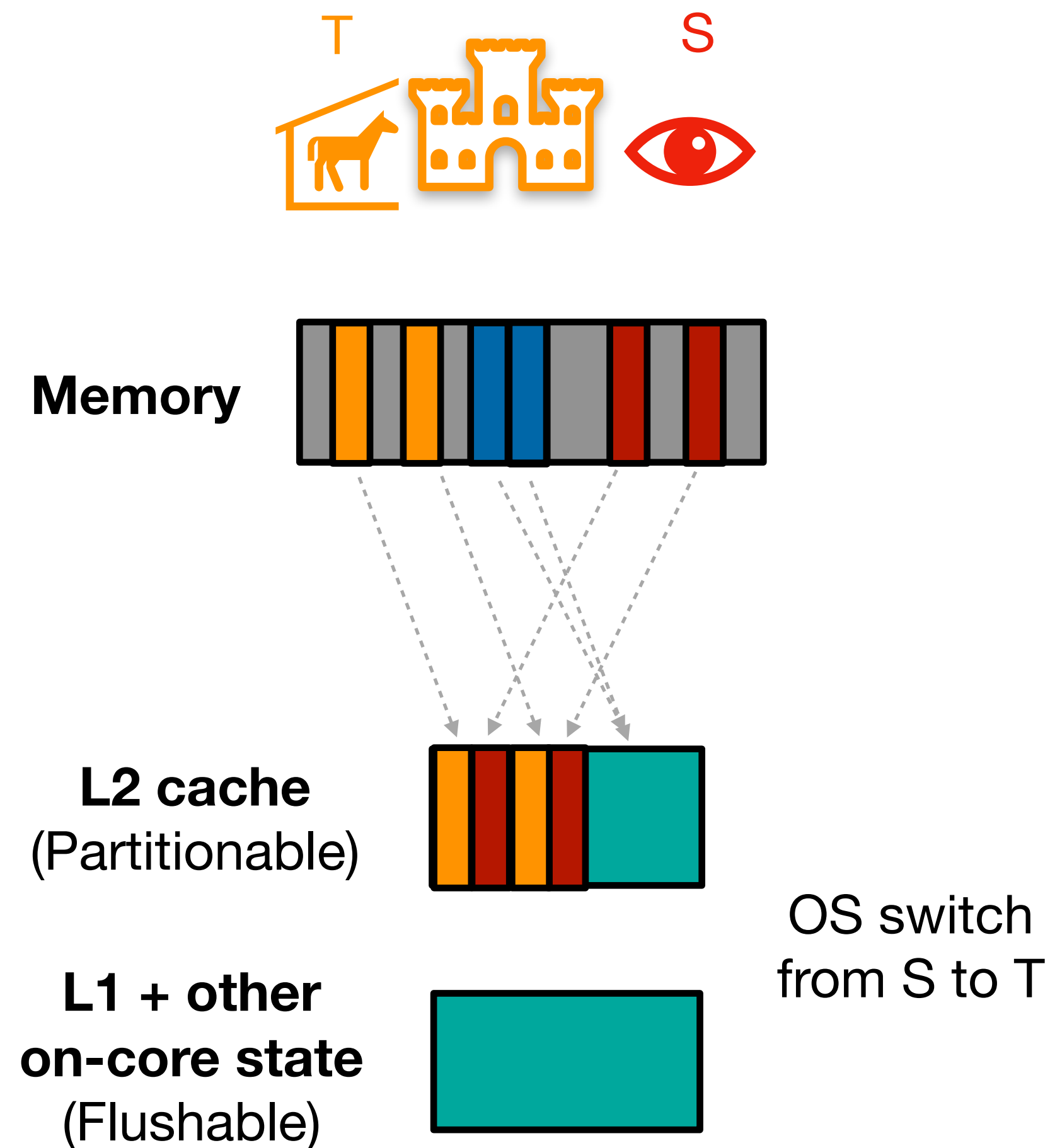
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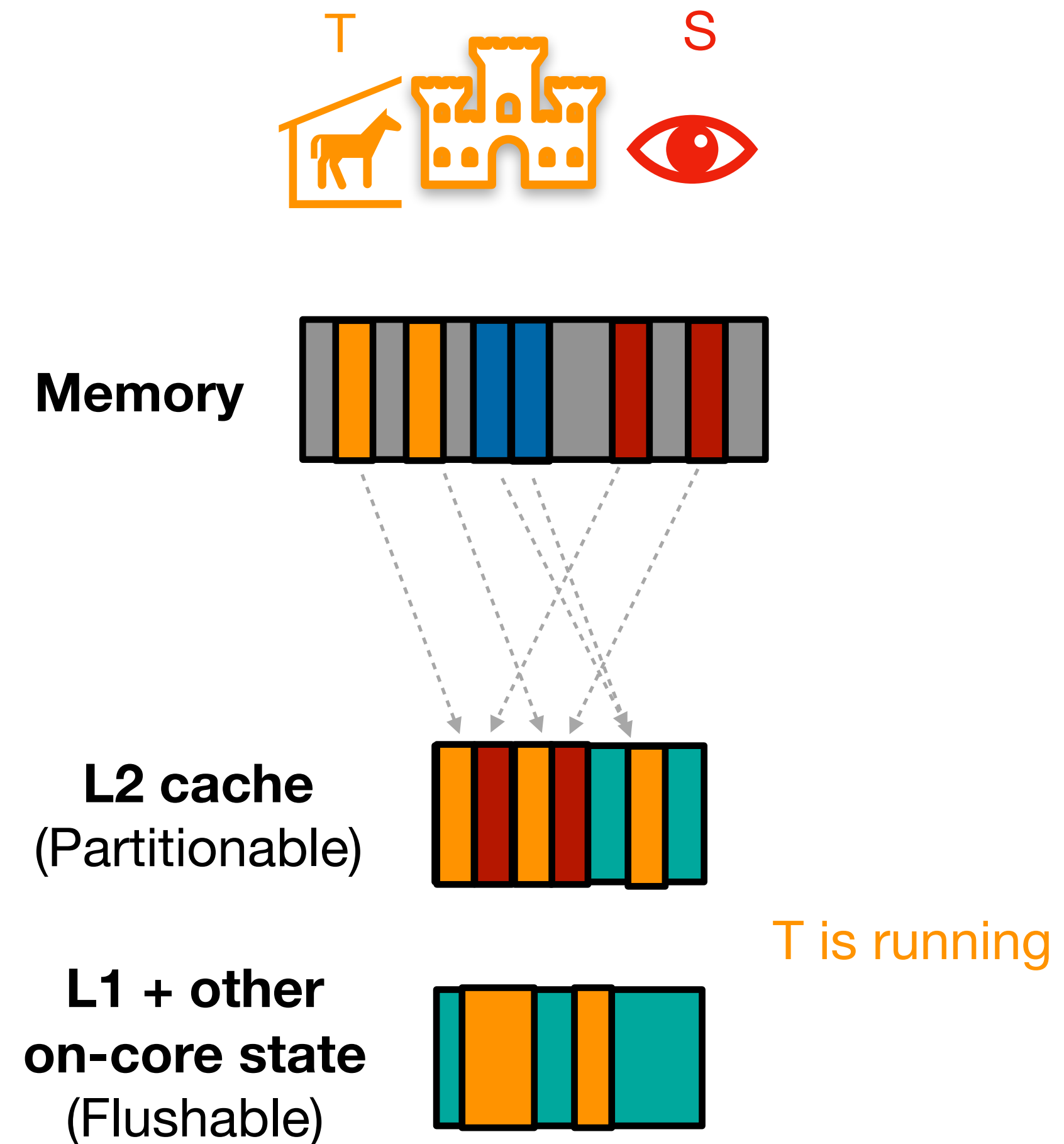
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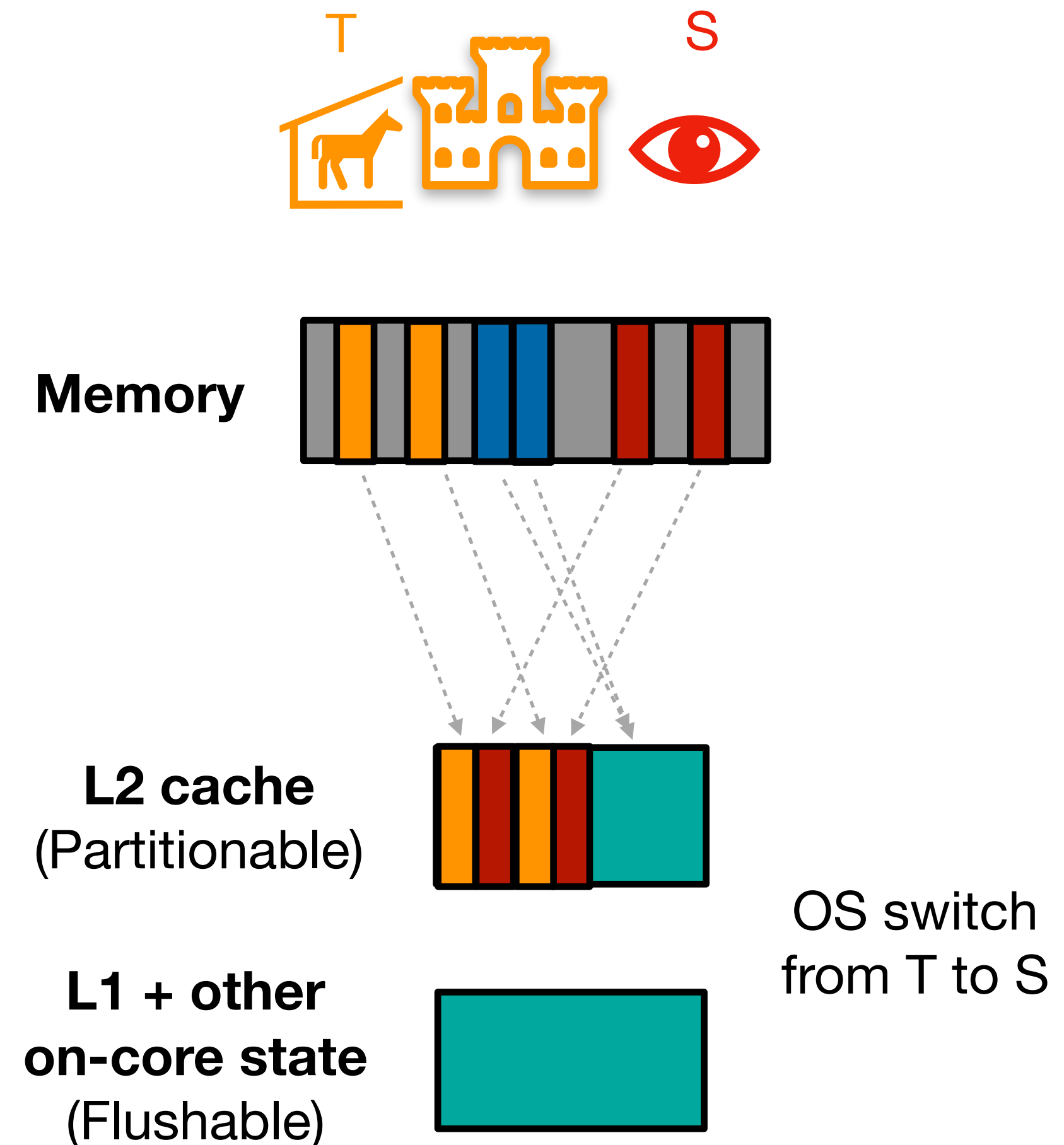
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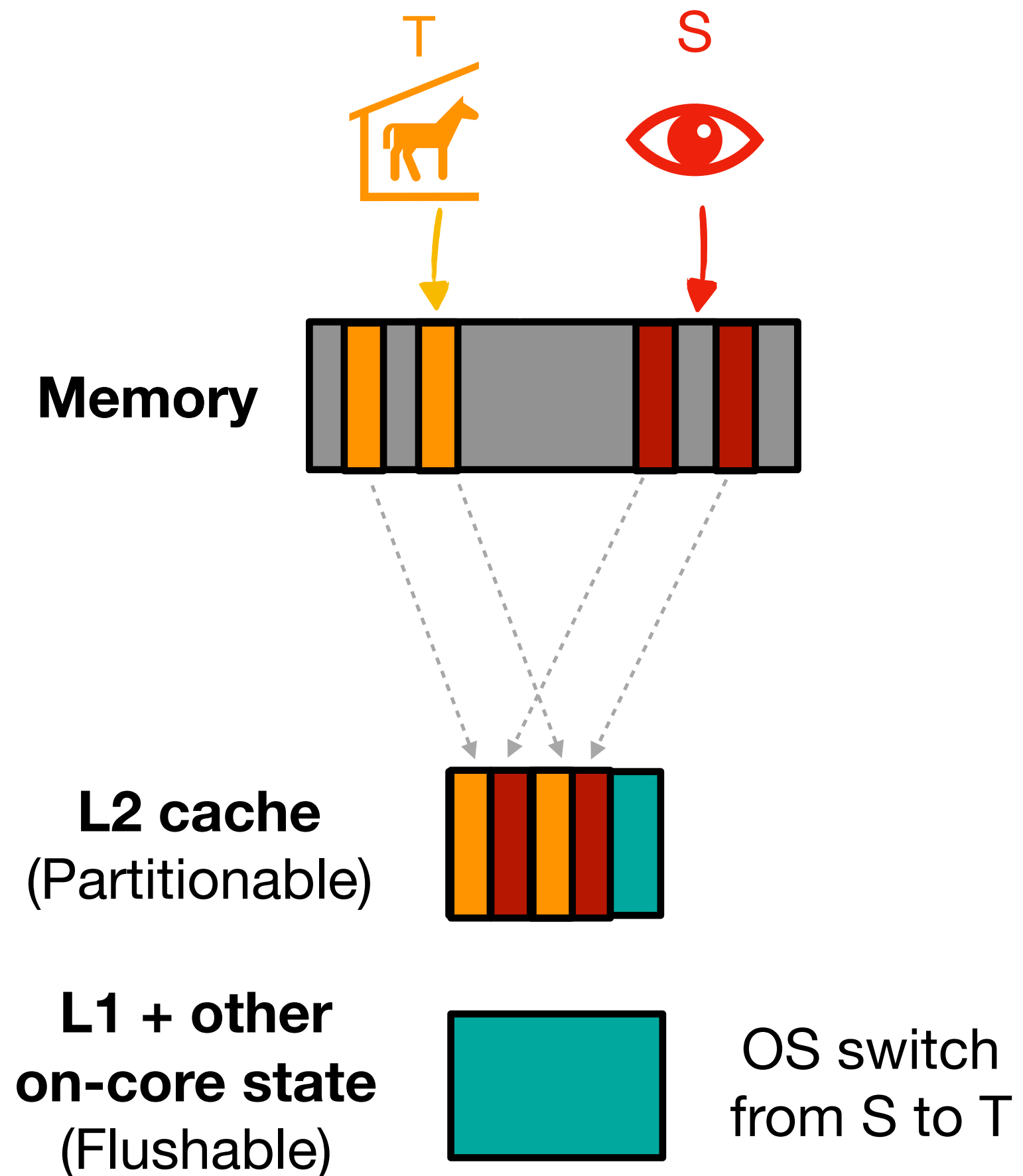


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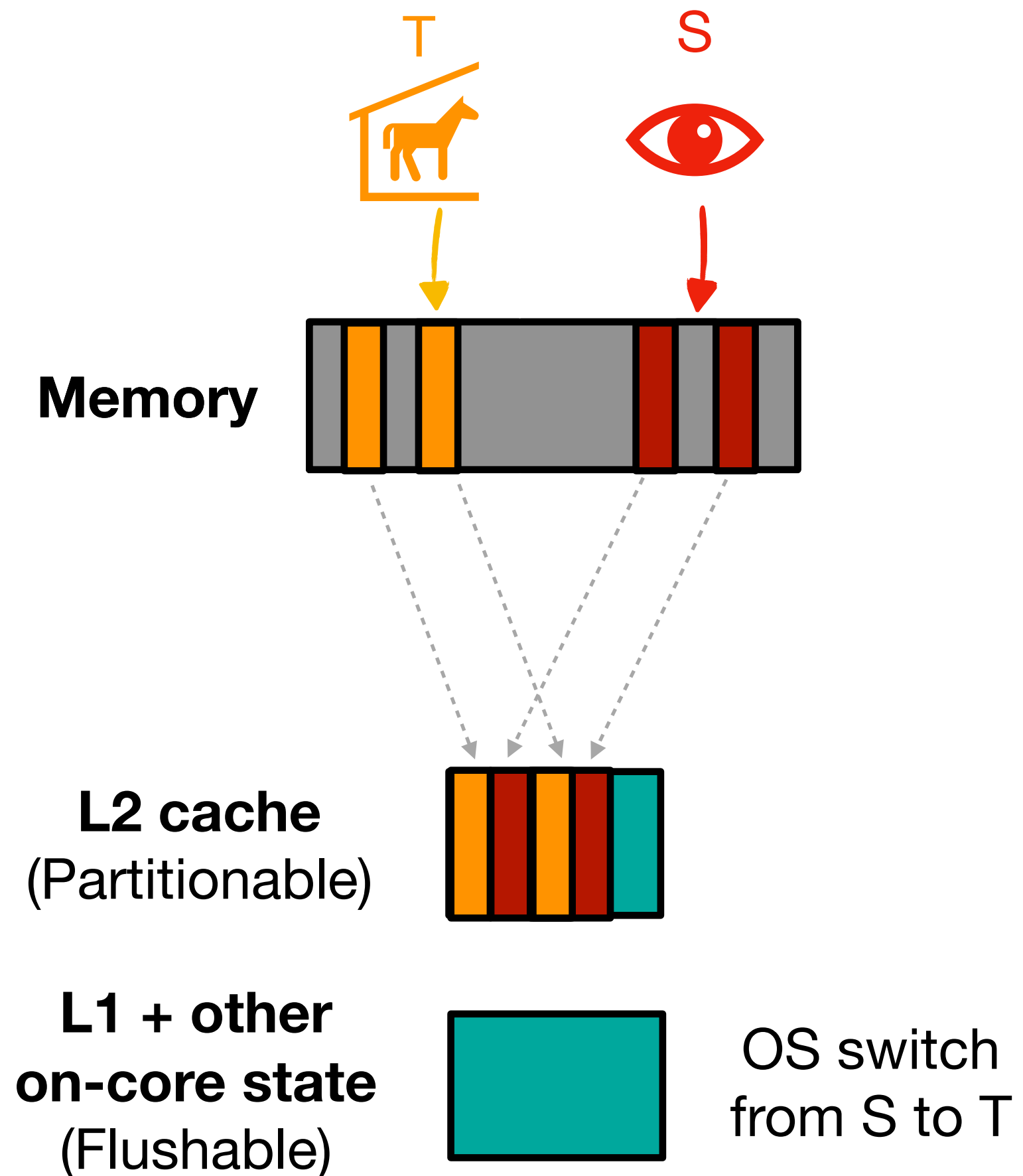


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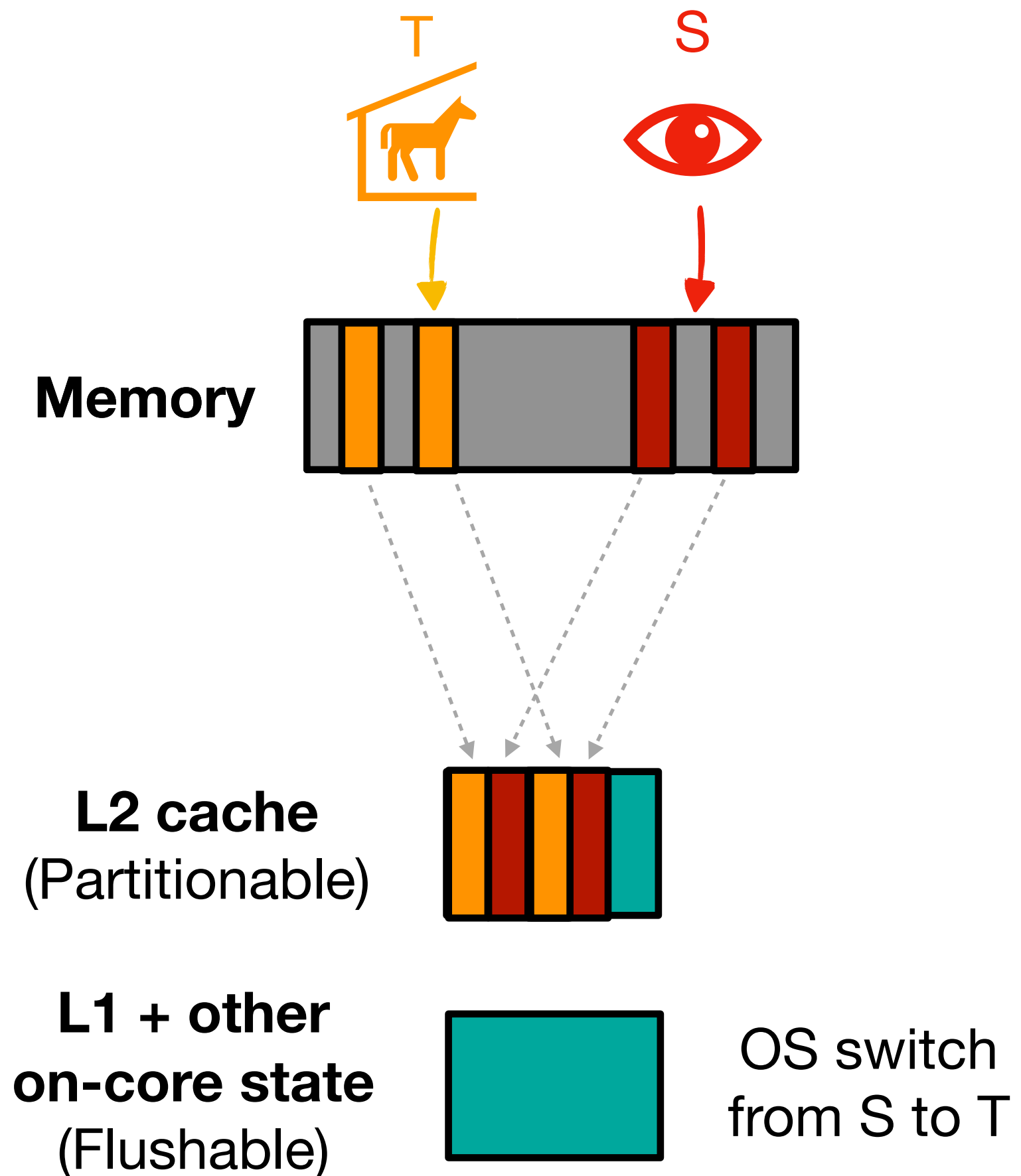
Qian Ge



Gernot Heiser

with
Yuval Yarom (U. Adelaide)
Tom Chothia (U. Birmingham)

seL4: World's first
OS kernel with
correctness proof!



“Flush”: Write fixed content; “Pad”: Wait up to fixed time.

seL4 The seL4 kernel and Time Protection



- OSes can implement *time protection*:
See EuroSys: [Ge et al. 2019]
- *Partition* off-core memory caches
- *Flush* on-core and non-architected state
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(HW support by [Wistoff et al. 2023])

seL4: World's first
OS kernel with
correctness proof!



Scott Buckley



Rob Sison



Nils Wistoff



Curtis Millar



Toby Murray



Gerwin Klein



Gernot Heiser

Thanks to funding from
Australian Research Council

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- **This talk (pt I):** How do we verify it works?

seL4: World's first
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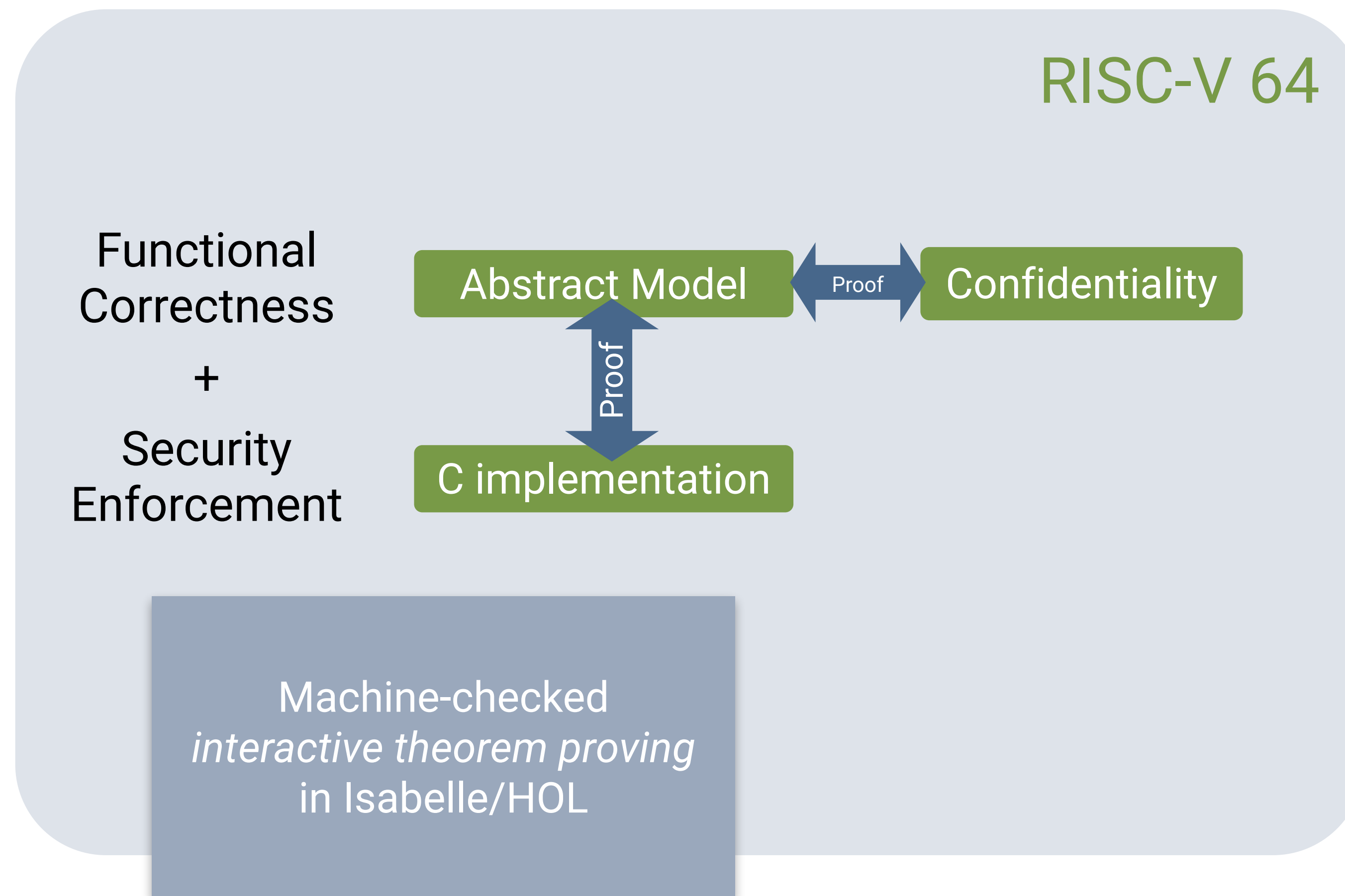
Gernot Heiser

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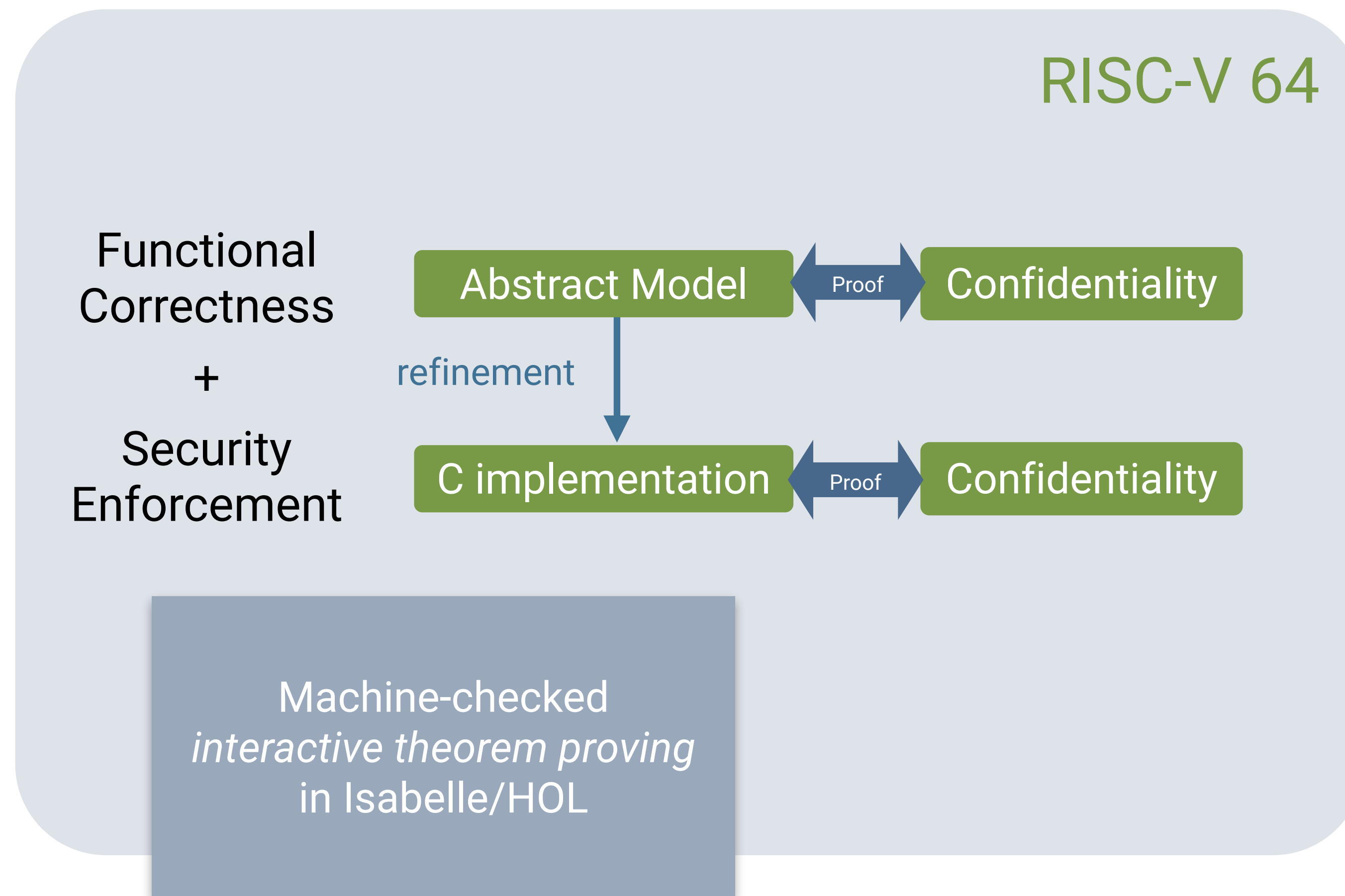


Time protection verification for seL4



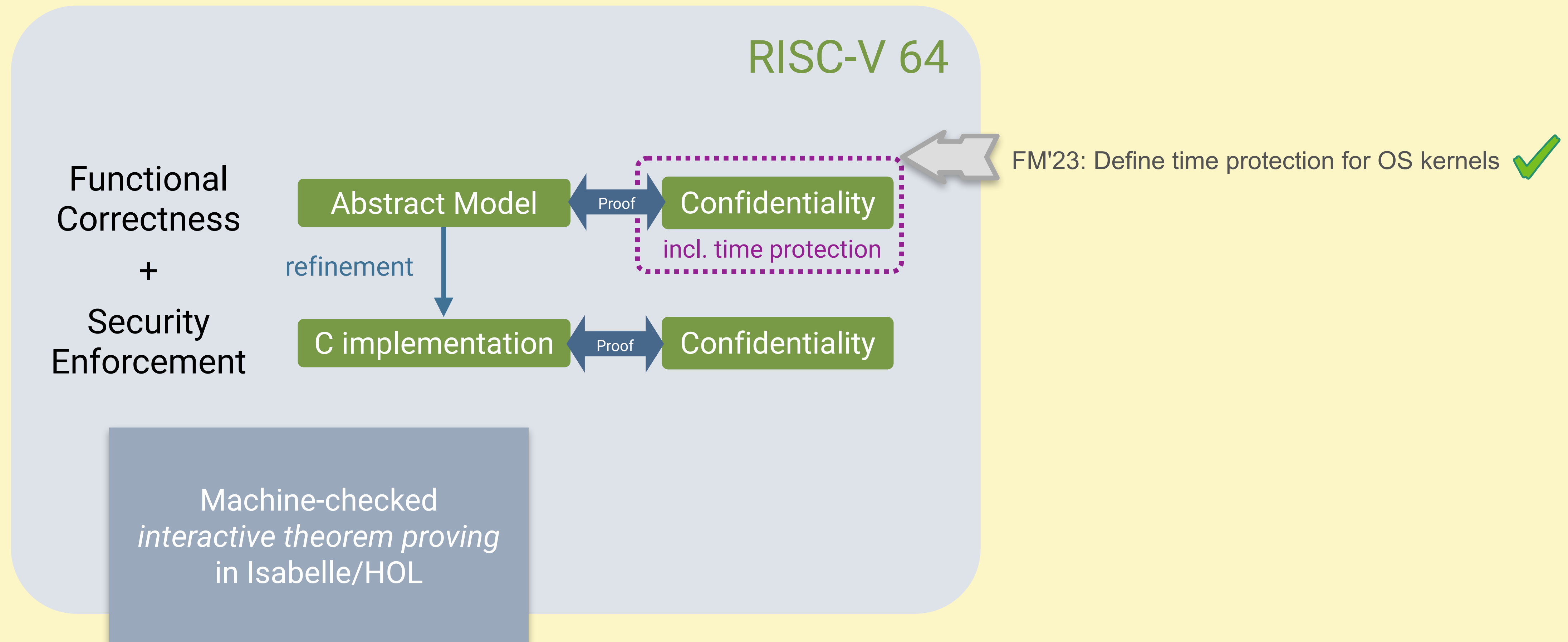


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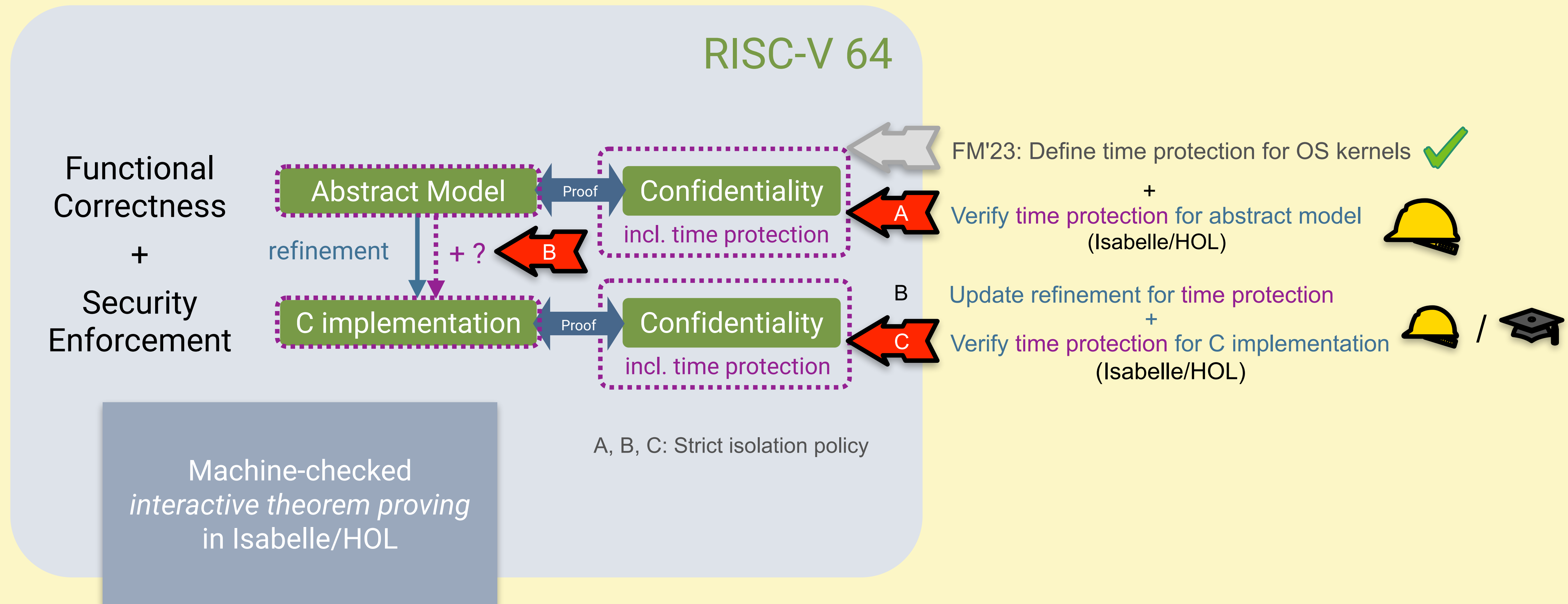
The plan 2 years ago...

Thanks to funding from
Australian Research Council



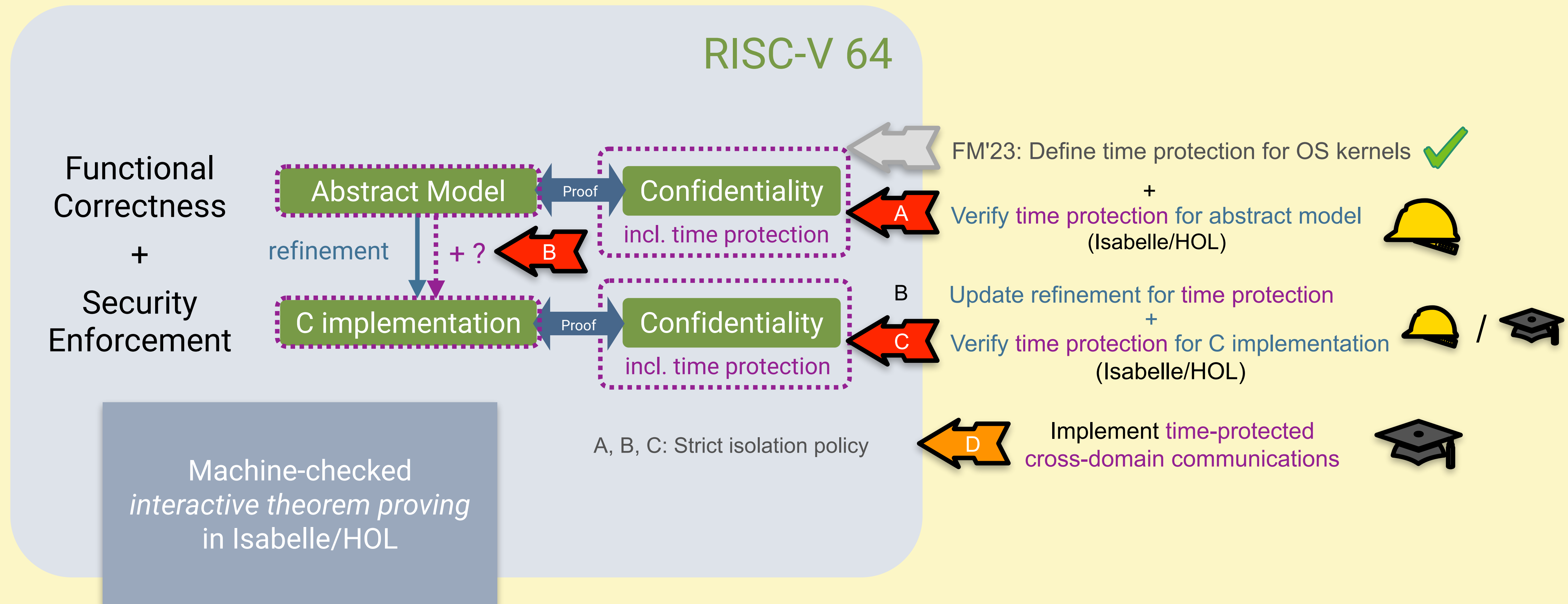
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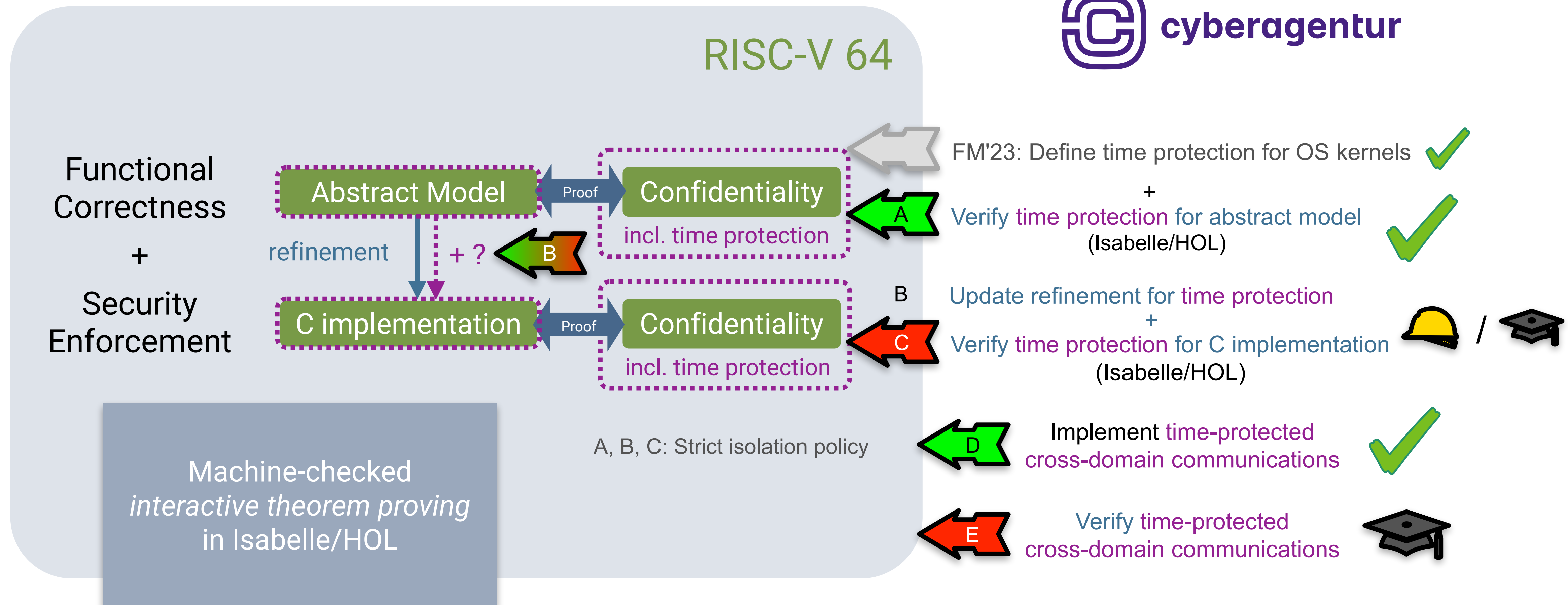


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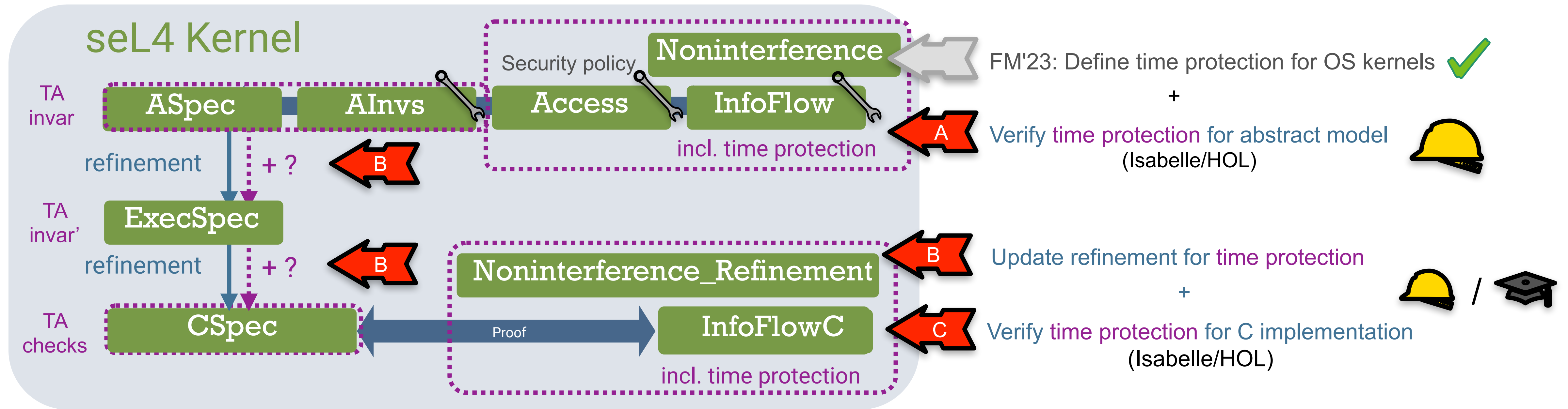


The status today:

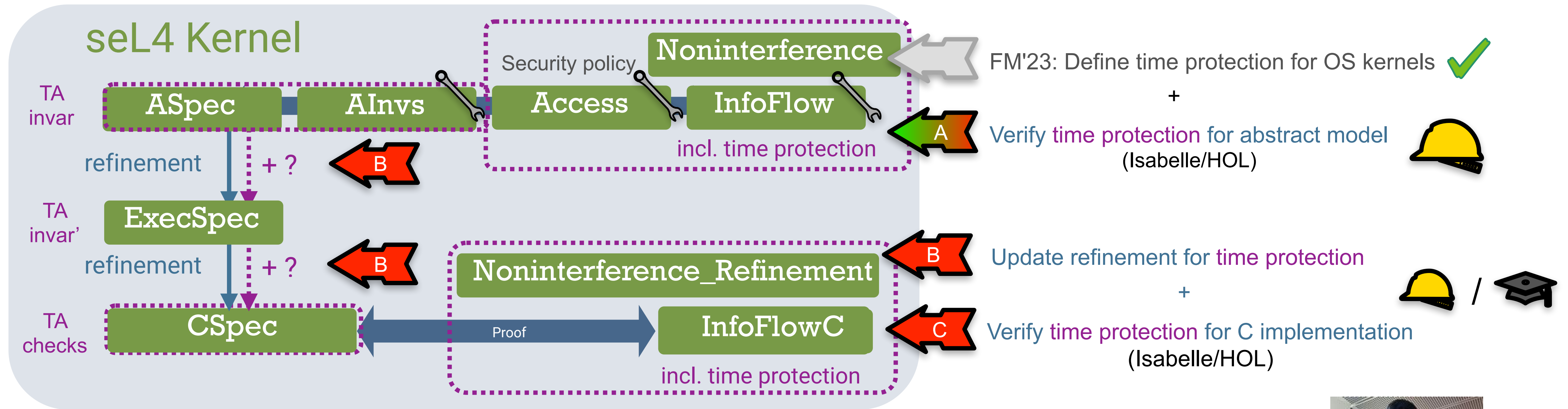
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Time protection verification for seL4



Time protection verification for seL4

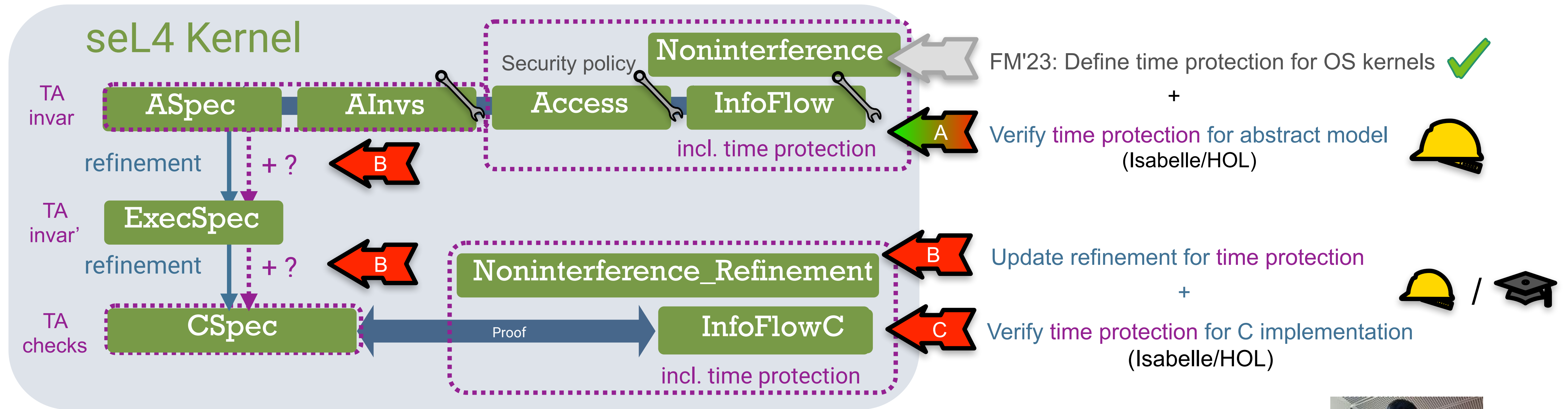


- (A) Key ASpec property: “TA invariant”

Sai Nair
BSc(Hons)
thesis



Time protection verification for seL4



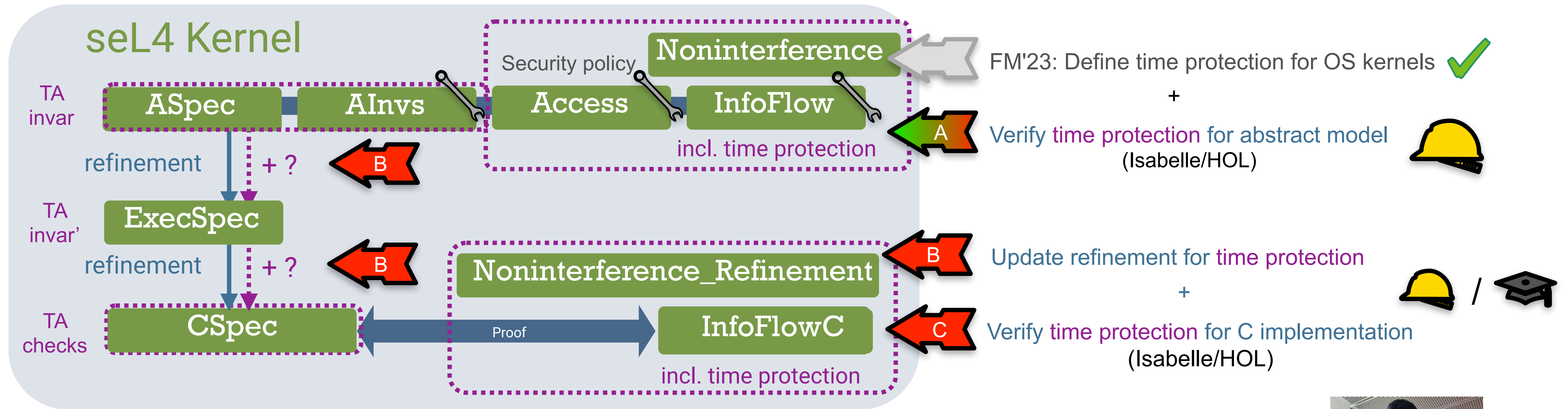
“obj refs don’t point outside static TA set”

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Sai Nair
BSc(Hons)
thesis



Time protection verification for seL4



"obj refs don't point outside static TA set"

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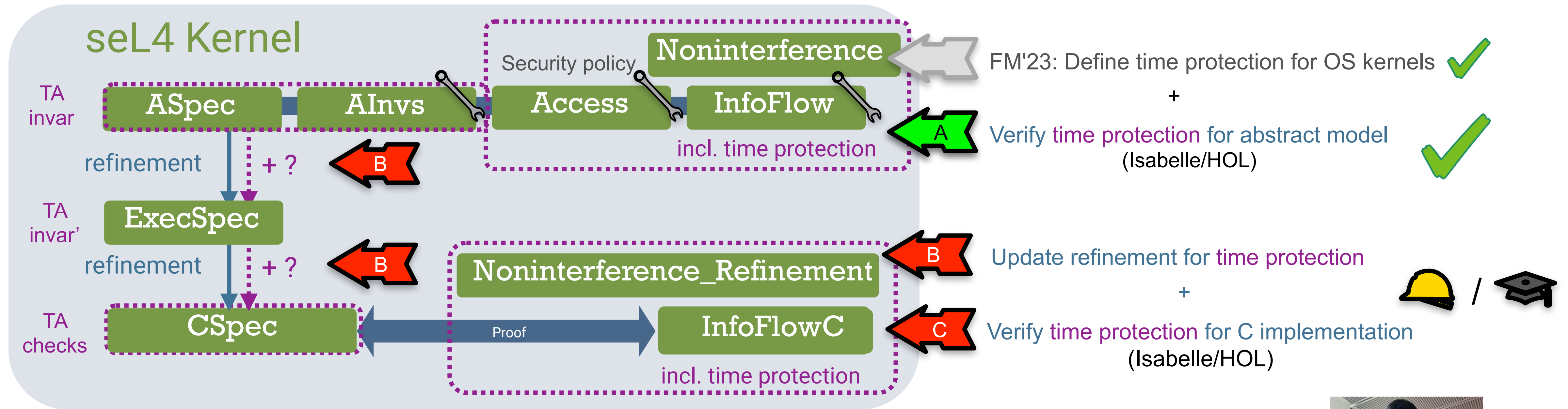
- Proof across **ASpec** in progress

Continuing on from

Sai Nair
BSc(Hons)
thesis



Time protection verification for seL4



“obj refs don’t point outside static TA set”

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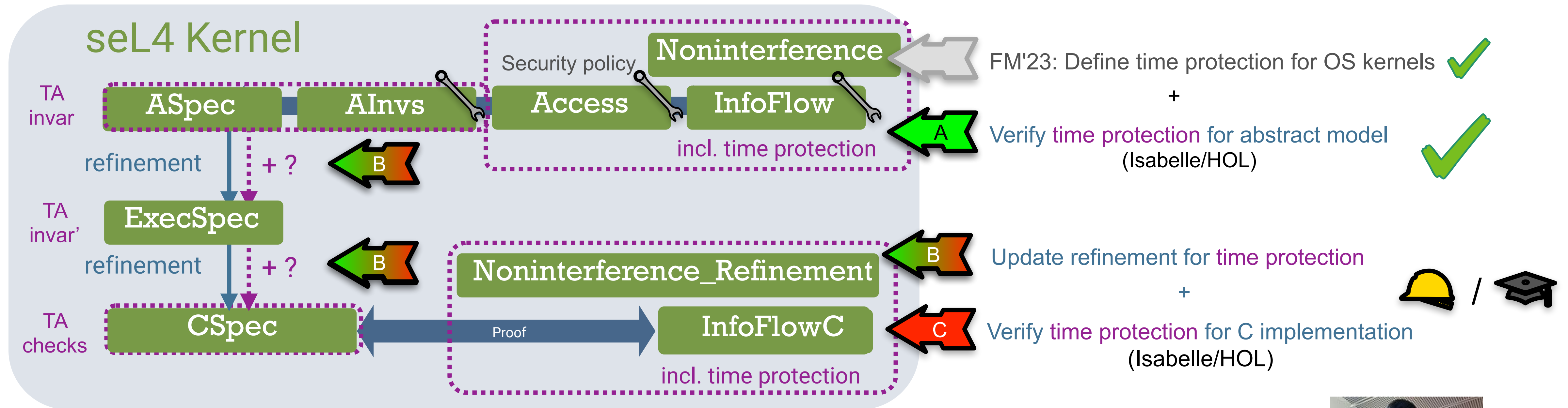
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Continuing on from

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BSc(Hons)
thesis



Time protection verification for seL4



“obj refs don’t point outside static TA set”

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Continuing on from

Sai Nair
BSc(Hons)
thesis



- (B + C) Refinement: TA invariant (via **ExecSpec**) $\Rightarrow$ TA checks pass (**CSpec**)

Continuing on from

Thomas Liang
BSc (Hons)
Thesis





Time-protected communications in seL4



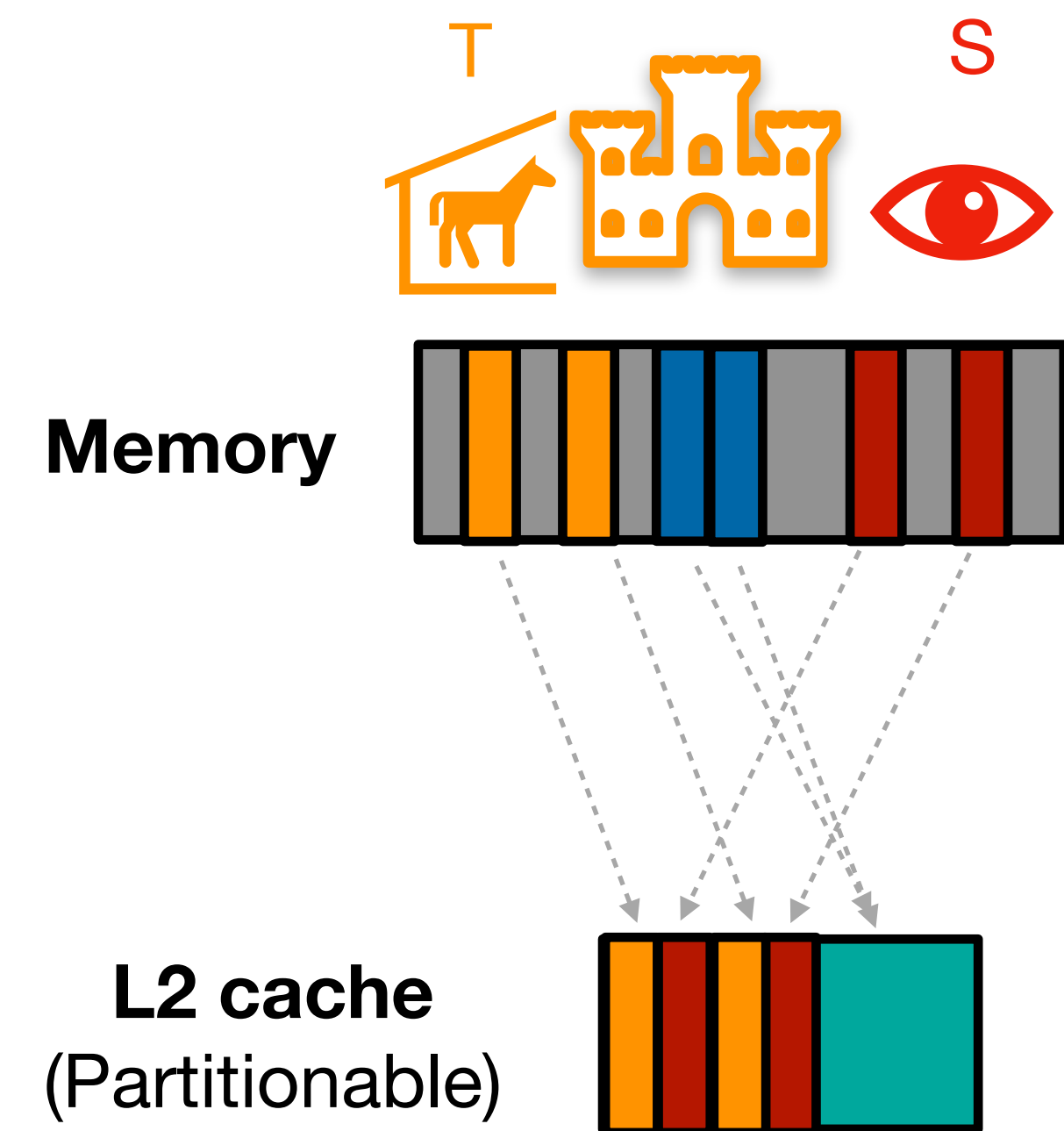
seL4 on RISC-V



Implement time-protected cross-domain communications



Verify time-protected cross-domain communications



We need *targeted flush* for partitionable L2 caches to enforce $T \not\sim S$ while allowing $T \sim S$

seL4 Time-protected communications in seL4



seL4 on RISC-V



Implement time-protected cross-domain communications



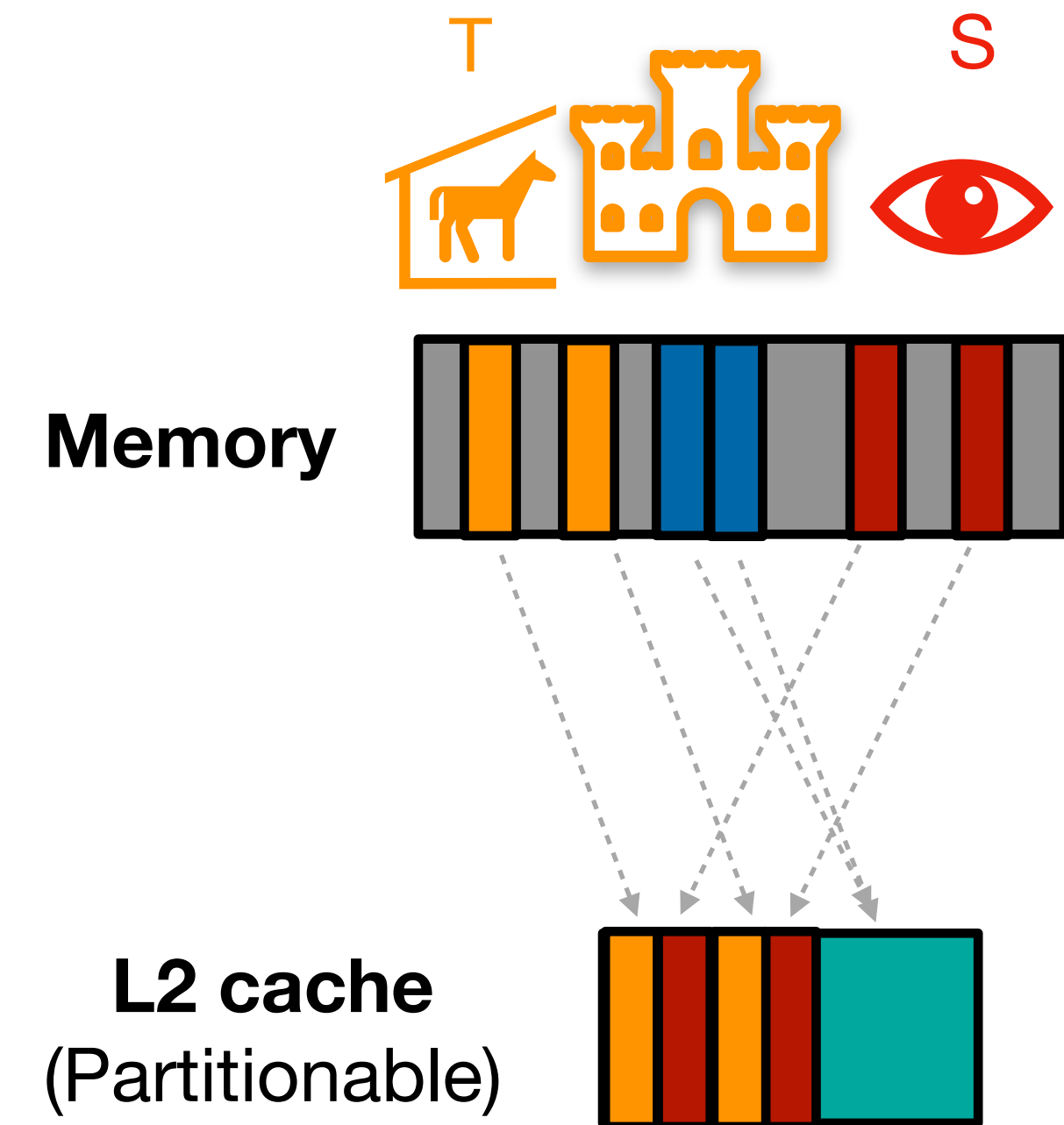
Verify time-protected cross-domain communications



- [Sethu 2025] comprehensively evaluated “legacy” implementation options on seL4, with the L2 partitioned via *cache colouring*:



Varun Sethu
BE Thesis



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seL4 on RISC-V



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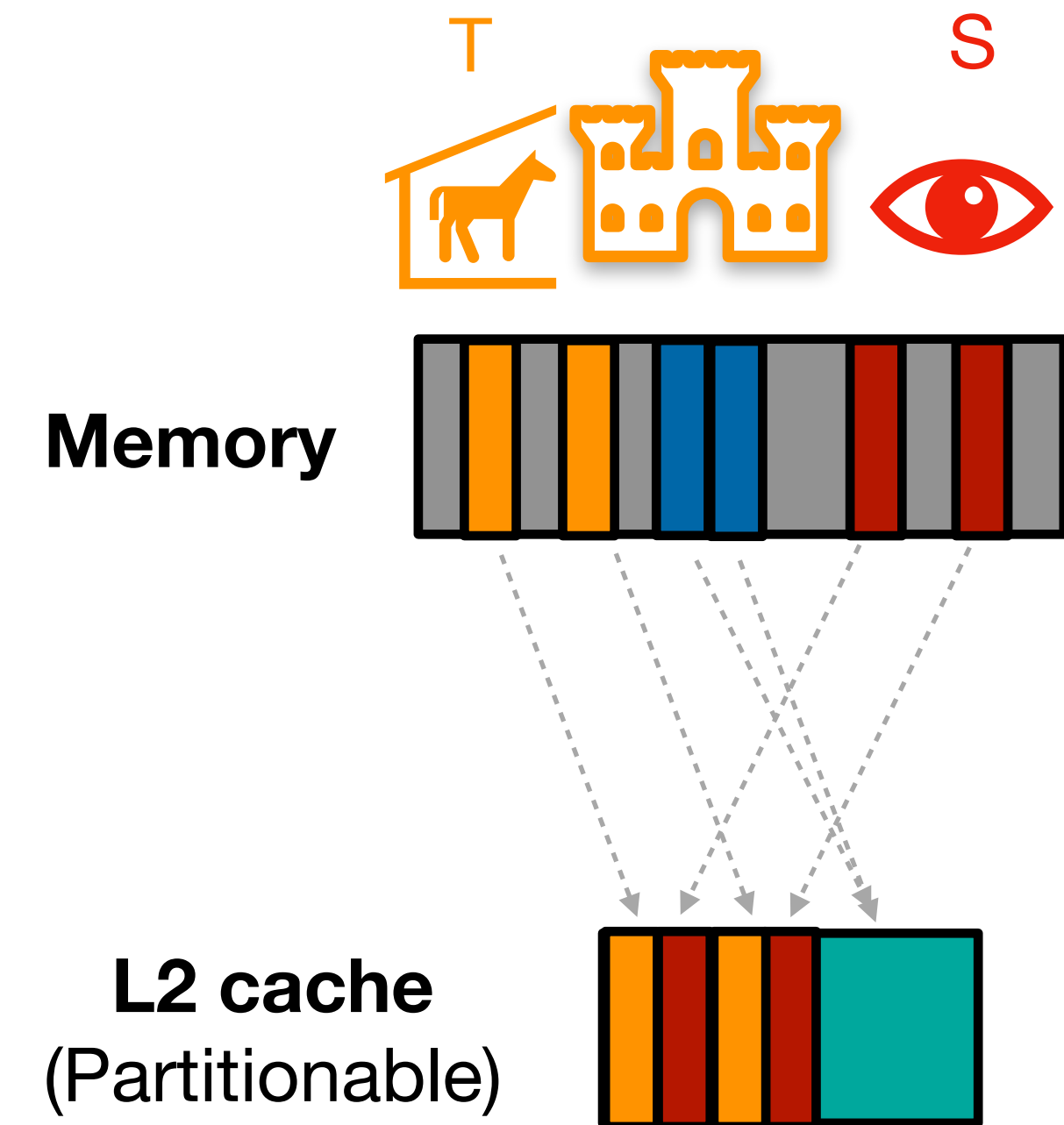
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seL4 Time-protected communications in seL4



seL4 on RISC-V



Implement time-protected cross-domain communications



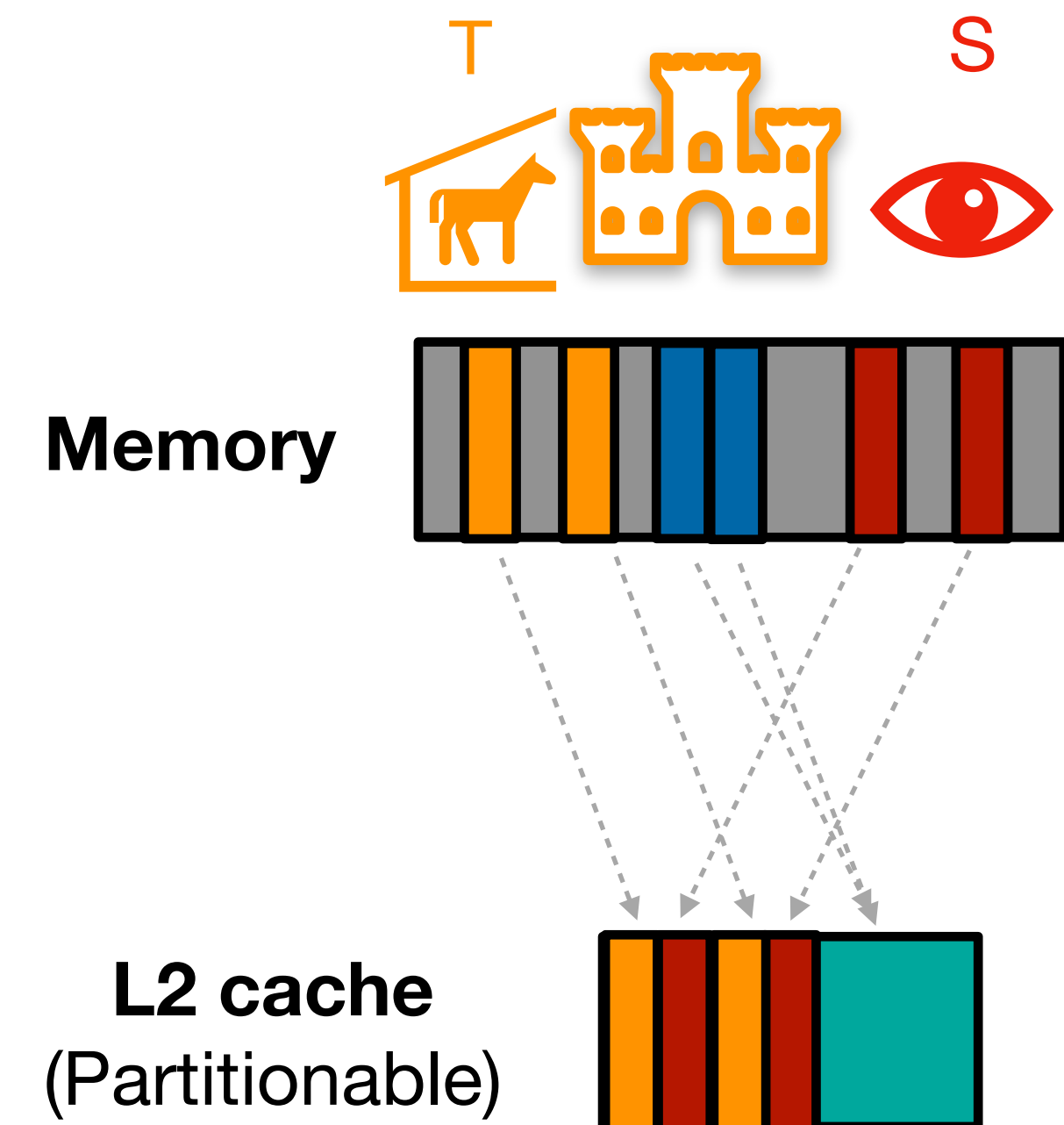
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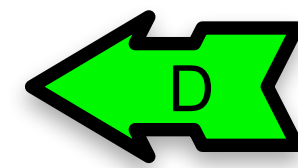


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seL4 Time-protected communications in seL4



seL4 on RISC-V



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Verify time-protected cross-domain communications

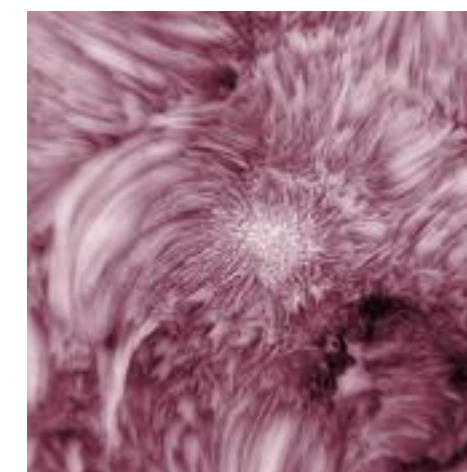


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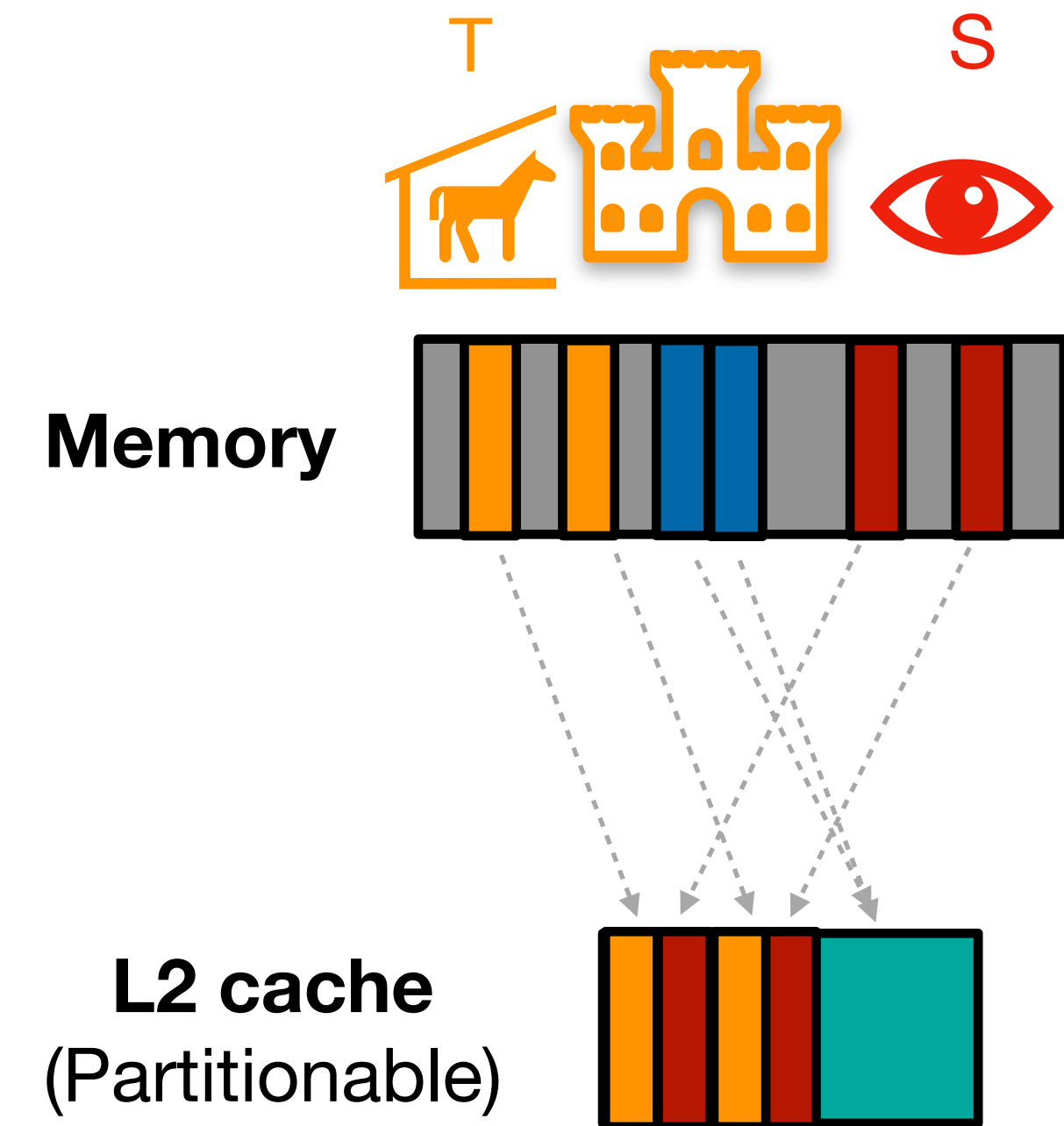
Continuing on from



Varun Sethu
BE Thesis



Julia Vassiliki

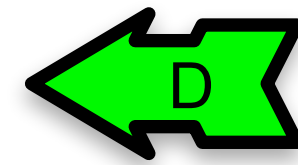


We need *targeted flush* for partitionable L2 caches to enforce $T \not\sim S$ while allowing $T \sim S$

seL4 Time-protected communications in seL4



seL4 on RISC-V



Implement time-protected cross-domain communications



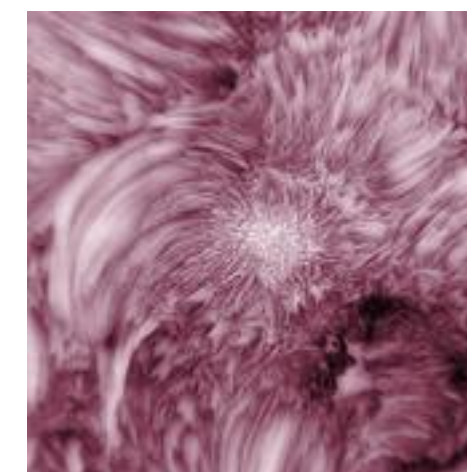
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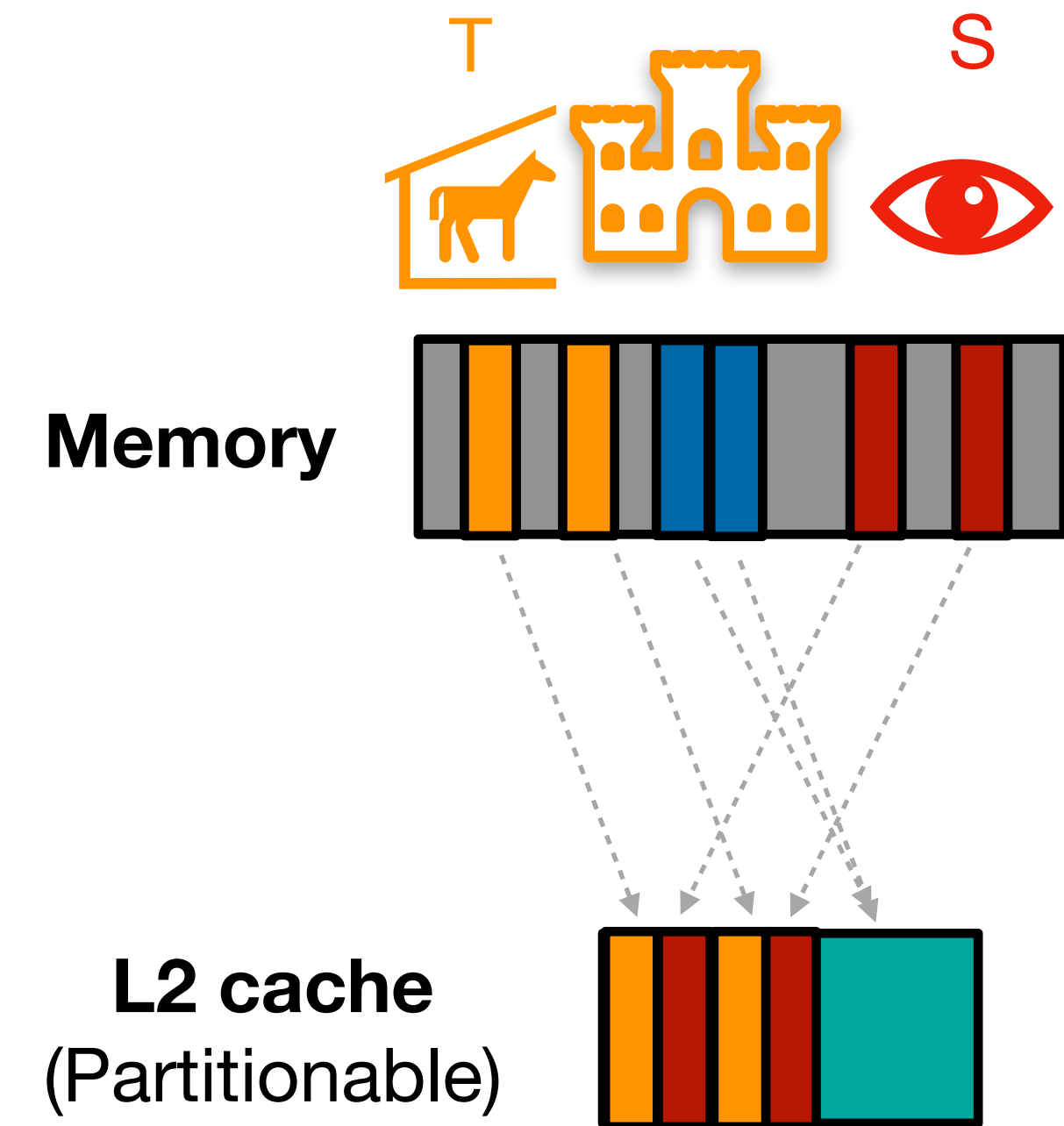
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 - Supports *targeted flush* of partitions
 - Adding needed *time padding* on flush



Varun Sethu
BE Thesis



Julia Vassiliki



We need *targeted flush* for partitionable L2 caches to enforce $T \not\sim S$ while allowing $T \sim S$

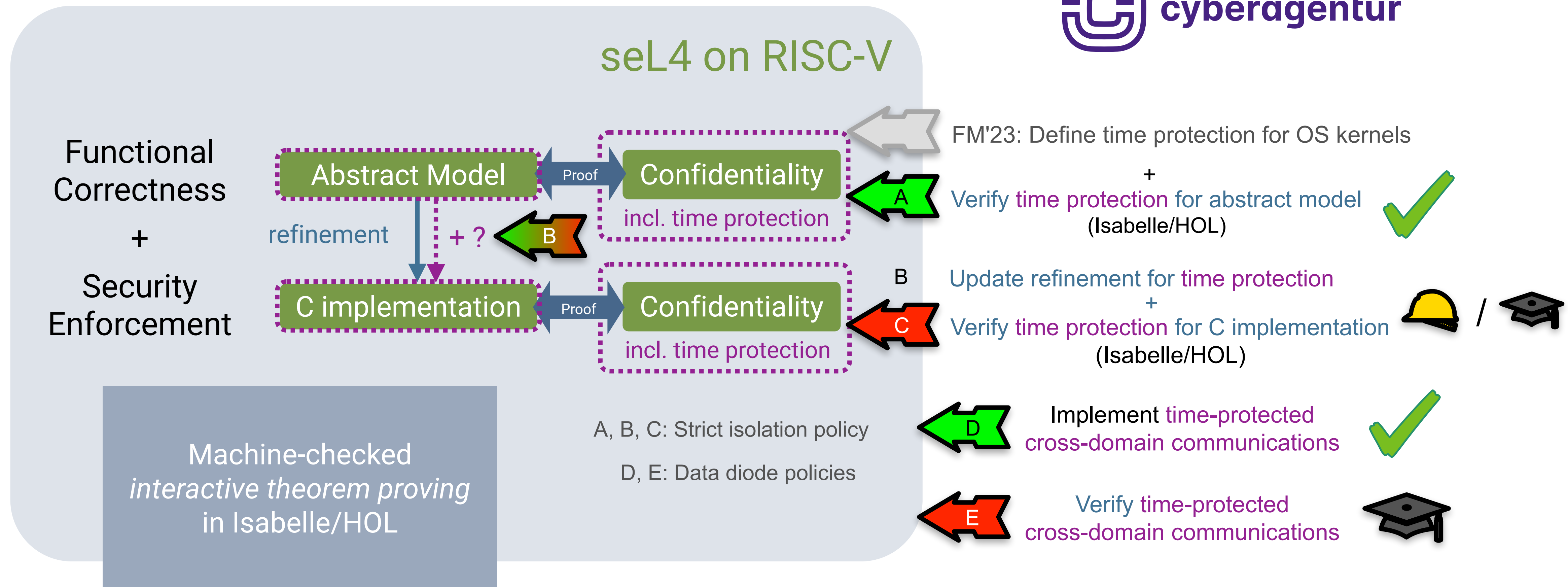


Time protection verification for seL4



The status today:

Thanks to funding from

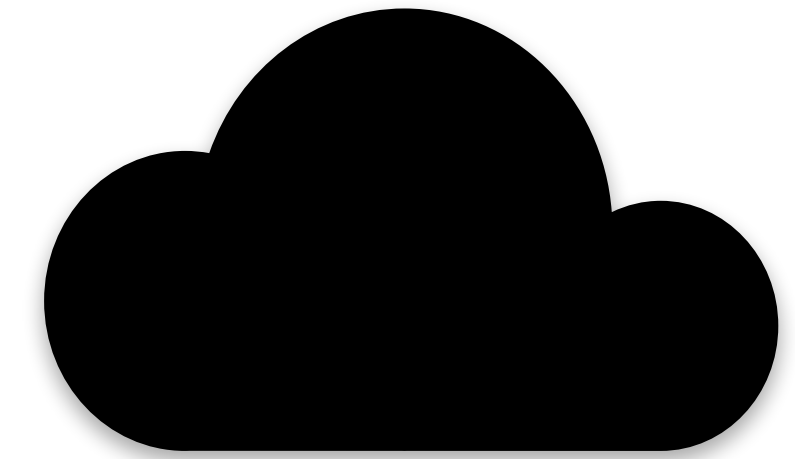


II: Kernel–Userland Gap



seL4: World's first
OS kernel with
correctness proof!

Question:





seL4: World's first
OS kernel with
correctness proof!



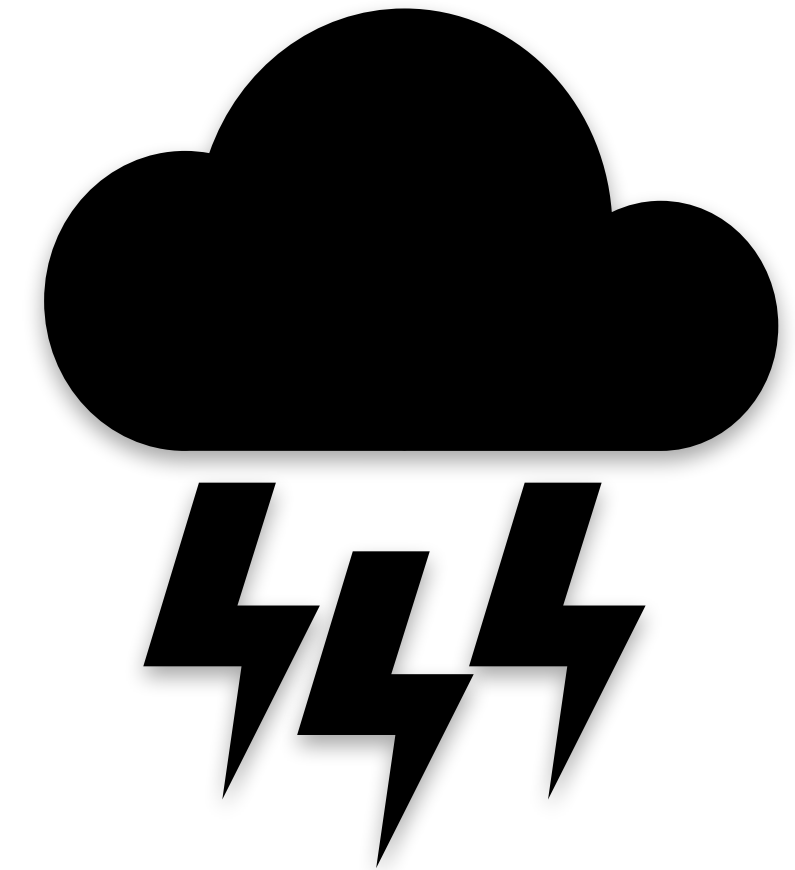
Question:
What do we mean when we say
“seL4 is **functionally correct**”?



seL4: World's first
OS kernel with
correctness proof!

Question:

What do we mean when we say
“seL4 is **functionally correct**”?



Claim:

seL4 has *not* been proved **functionally correct**
enough to verify its users!

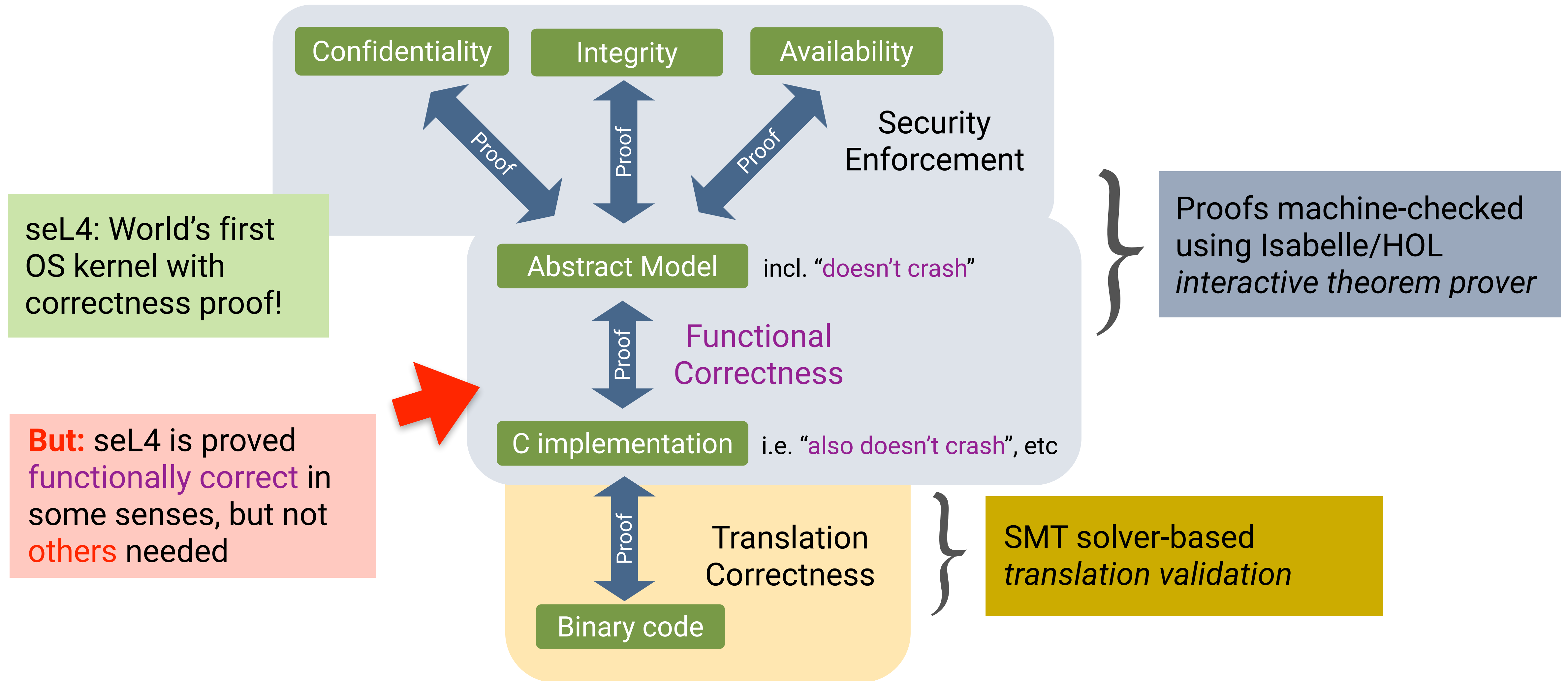


The verified seL4 OS microkernel

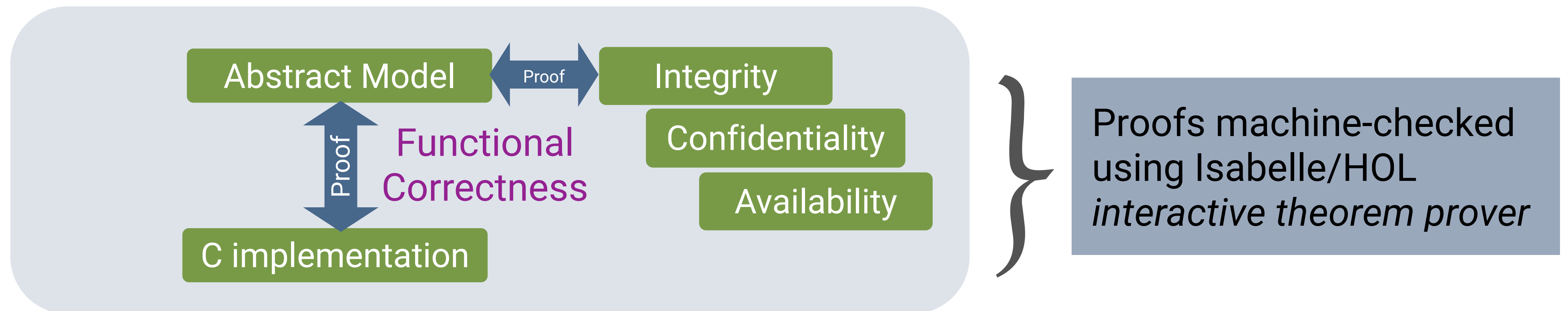


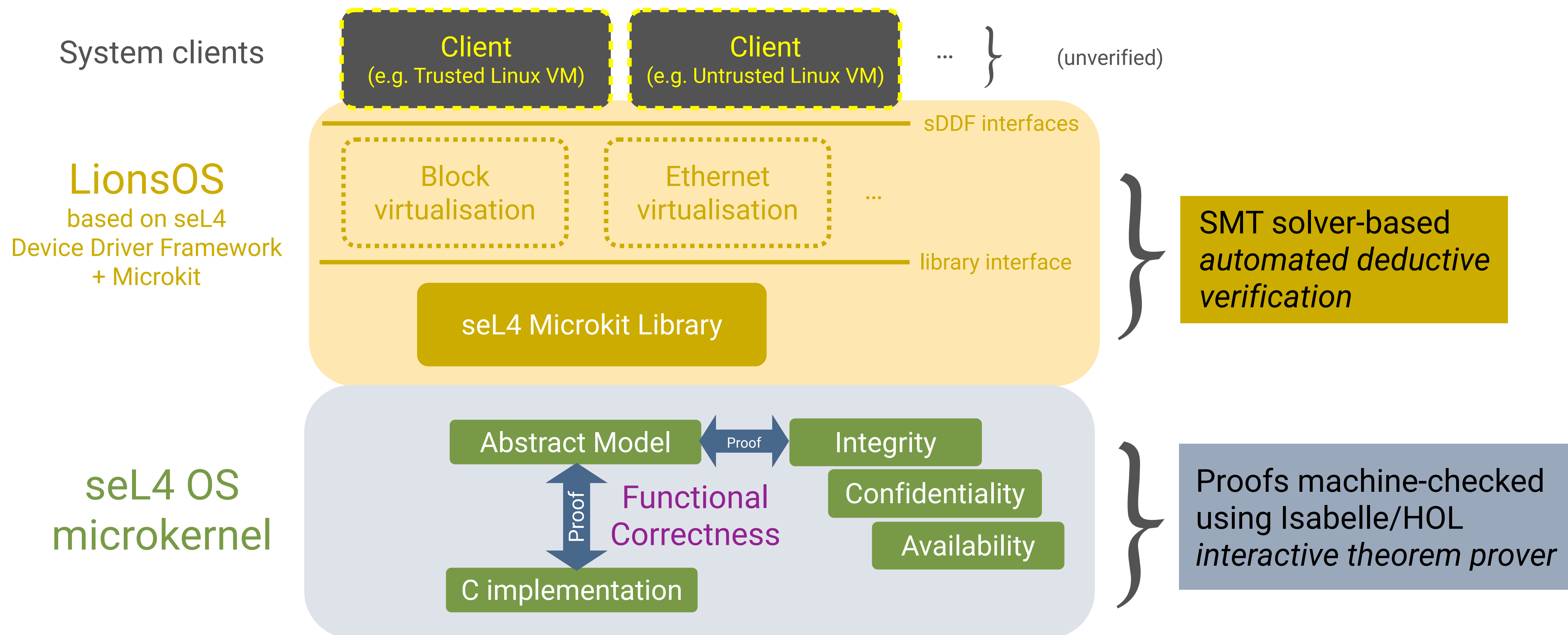
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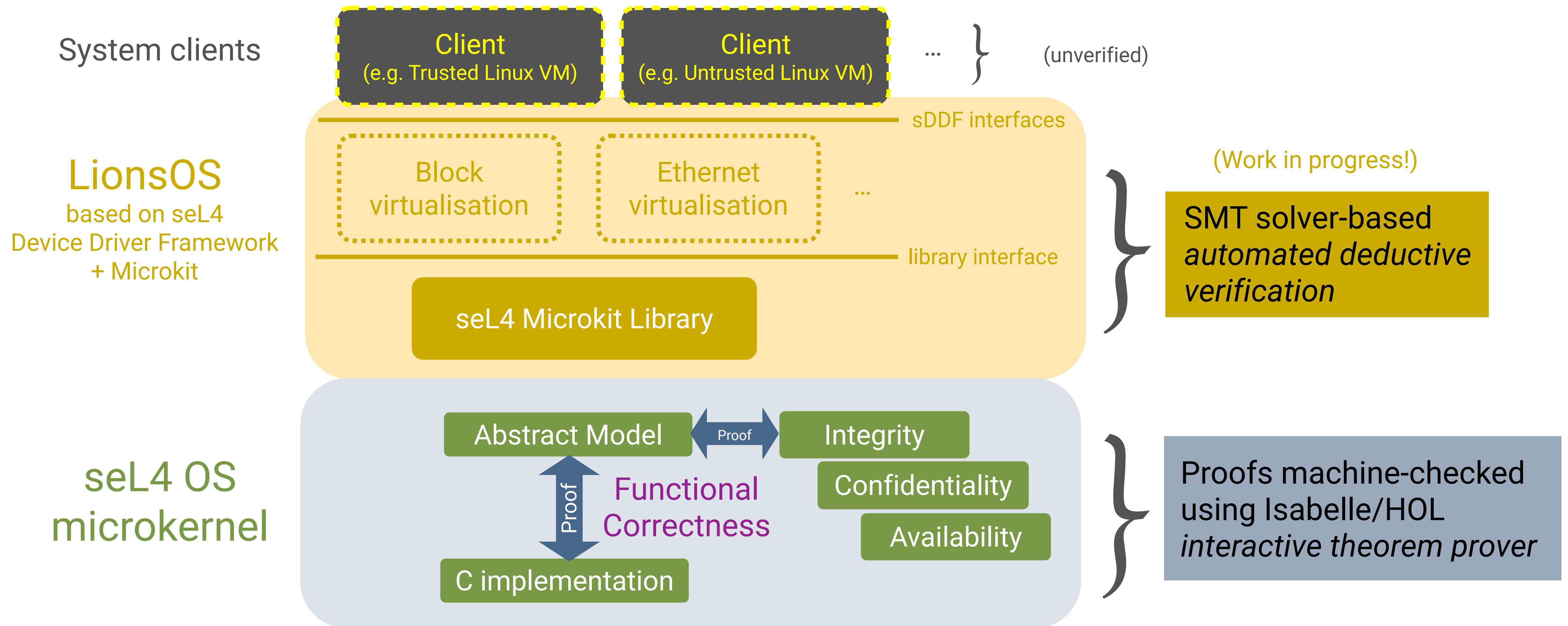
But: seL4 is proved
functionally correct in
some senses, but not
others needed

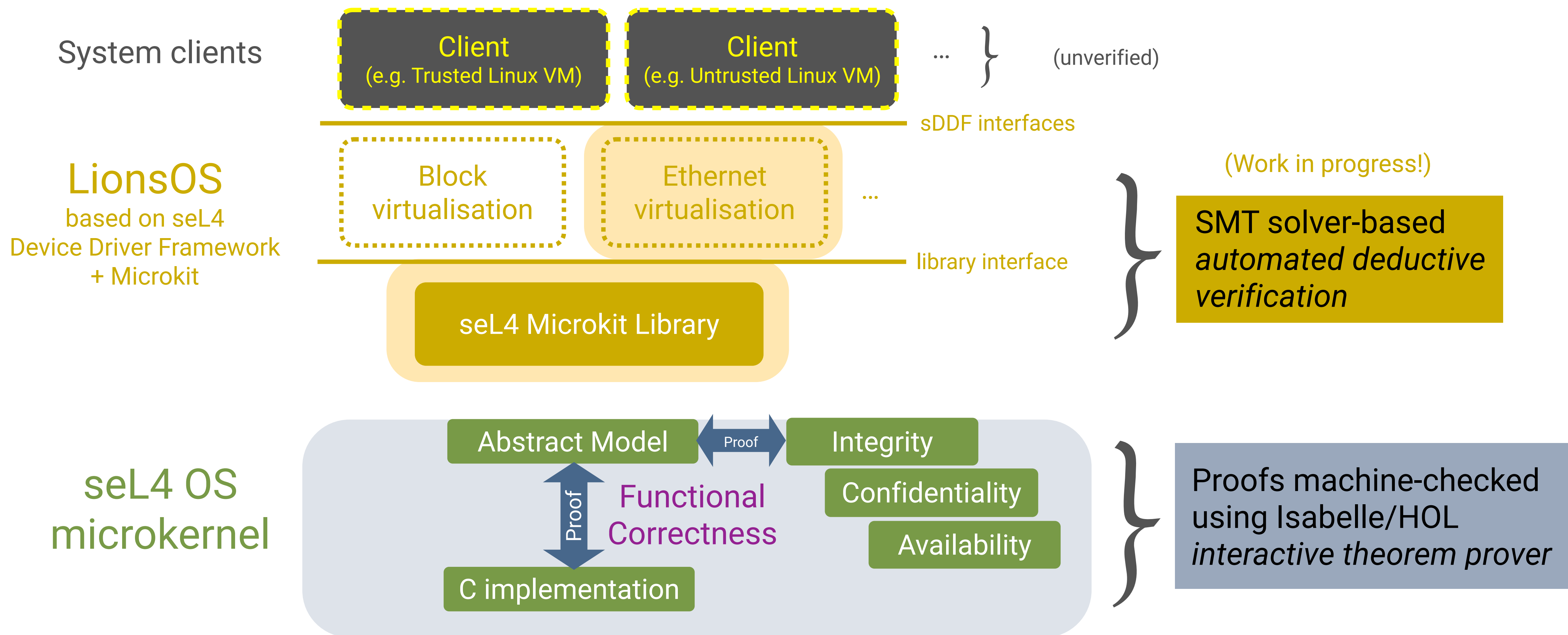


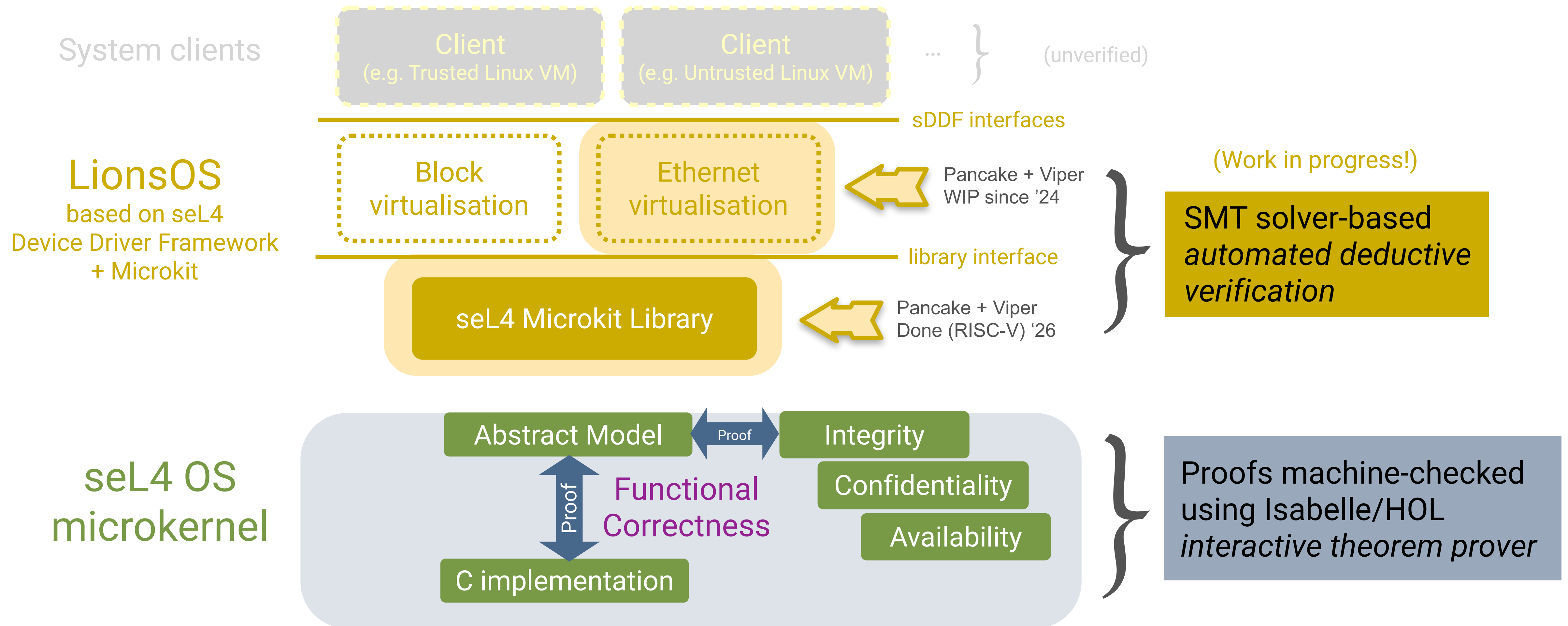
seL4 OS
microkernel

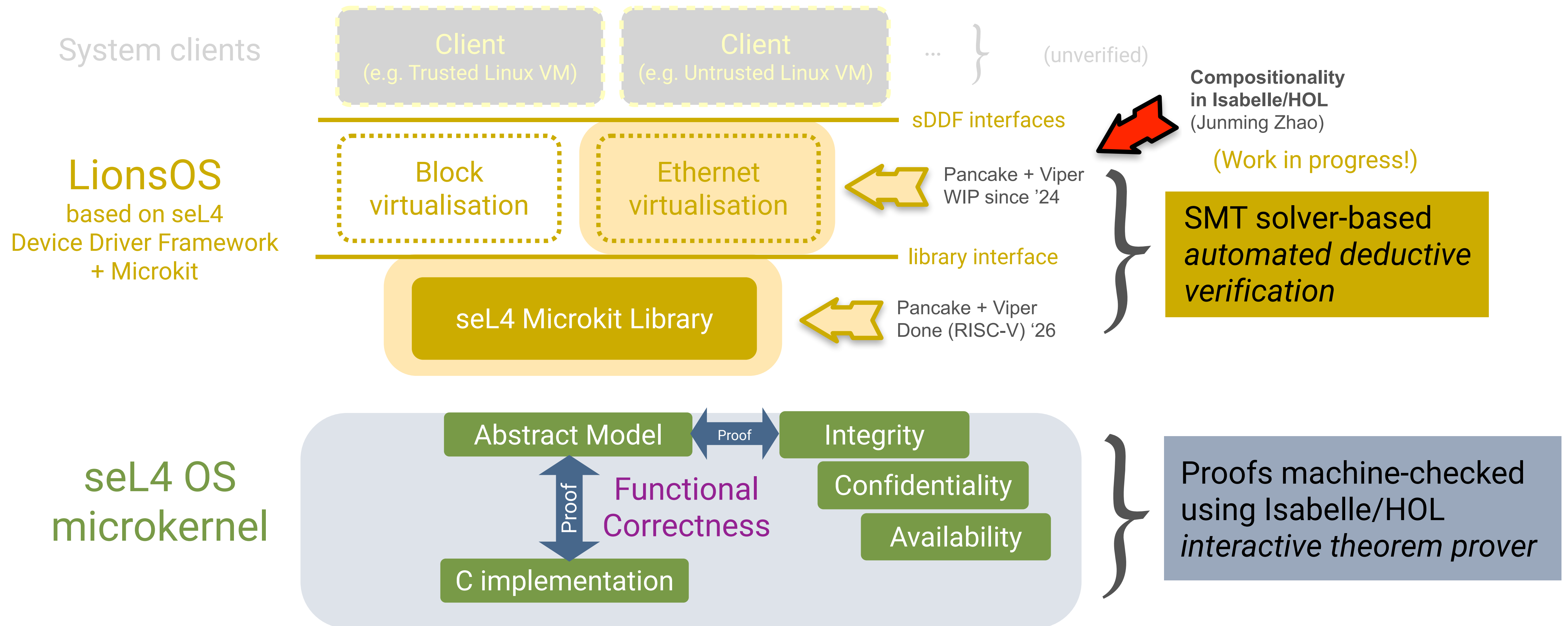


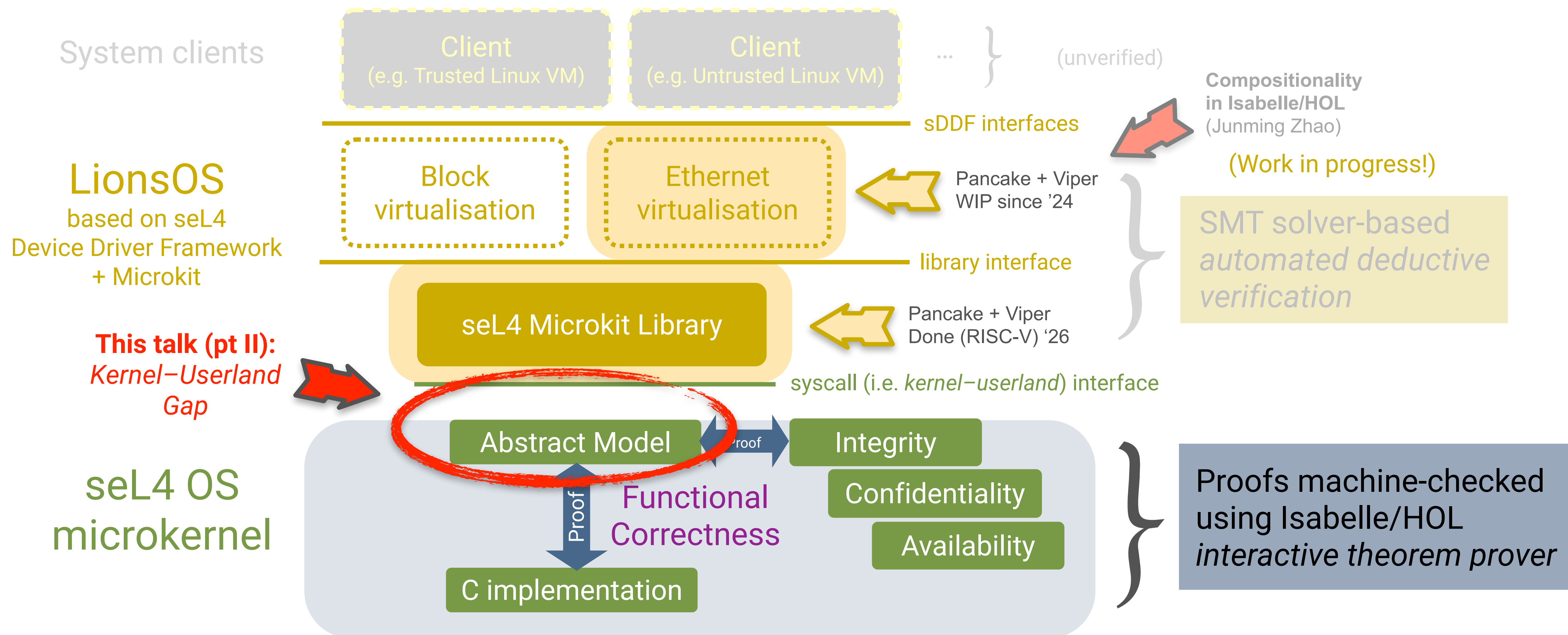












seL4 Microkit assumes seL4's syscalls work



```
static void handler_loop(void) {
```

```
...
```

```
    if (have_reply) {
```

```
        ...
```

```
    } else {
```

```
        tag = seL4_Recv(INPUT_CAP, &badge, REPLY_CAP);
```

```
    }
```

```
...
```

```
}
```

seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

seL4 Microkit assumes seL4's syscalls work



```
static void handler_loop(void) {
```

```
...  
  {{ R }} Precondition
```

```
  if (have_reply) {
```

```
    {{ R && ... }} ... {{ S }}
```

```
  } else {
```

```
    {{ R && ! have_reply && ! microkit_have_signal }}
```

```
    tag = seL4_Recv(INPUT_CAP, &badge, REPLY_CAP);
```

```
    {{ S }}
```

```
  }
```

```
  {{ S }}
```

```
...  
} Postcondition
```

Hoare triples:
 $\{\{ \text{Pre} \} \} f \{\{ \text{Post} \} \}$

seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

seL4 Microkit assumes seL4's syscalls work



```
static void handler_loop(void) {
```

```
...  
  {{ R }} ← Precondition
```

```
  if (have_reply) {
```

```
    {{ R && ... }} ... {{ S }}
```

```
  } else {
```

Precond.

```
    {{ R && ! have_reply && ! microkit_have_signal }}
```

```
    // if  $R \ \&\& \ \dots \Rightarrow P$ , assume
```

```
    {{ P }}
```

```
    tag = seL4_Recv(INPUT_CAP, &badge, REPLY_CAP);
```

```
    {{ Q }}
```

```
    // if  $Q \Rightarrow S$ , conclude
```

Postcond.

```
    {{ S }}
```

```
  }
```

```
  {{ S }}
```

```
... ← Postcondition
```

```
}
```

Hoare triples:
 $\{\{ \text{Pre} \} \} f \{\{ \text{Post} \} \}$

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```
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```

```
...  
  {{ R }} Precondition
```

```
  if (have_reply) {
```

```
    {{ R && ... }} ... {{ S }}
```

```
  } else {
```

Precond.

```
    {{ R && ! have_reply && ! microkit_have_signal }}
```

```
    // if R && ... => P, assume
```

```
    {{ P }}
```

```
    tag = seL4_Recv(INPUT_CAP, &badge, REPLY_CAP);
```

```
    {{ Q }}
```

Postcond.

```
    // if Q => S, conclude
```

```
    {{ S }}
```

```
  }
```

```
  {{ S }} // done
```

```
...  
  Postcondition ✓
```

```
}
```

Hoare triples:
{{ Pre }} f {{ Post }}

seL4 Microkit Library

syscall (i.e. kernel-userland) interface

seL4 Microkit assumes seL4's syscalls work



But is it
true?

```
static void handler_loop(void) {  
  ...  
  {{ R }} Precondition  
  if (have_reply) {  
    {{ R && ... }} ... {{ S }}  
  } else {  
    {{ R && ! have_reply && ! microkit_have_signal }}  
    // if R && ... => P, assume  
    {{ P }}  
    tag = seL4_Recv(INPUT_CAP, &badge, REPLY_CAP);  
    {{ Q }}  
    // if Q => S, conclude  
    {{ S }}  
  }  
  {{ S }} // done  
  ... Postcondition   
}
```

Precond.  

Postcond. 

_____ syscall (i.e. kernel-userland) interface

Hoare triples:
 $\{\{ \text{Pre} \} \} f \{\{ \text{Post} \} \}$

seL4 Microkit Library

seL4 Microkit's assumptions need verifying!



```
static void handler_loop(void) { ...  
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    // if R && ... => P, assume  
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    // if Q => S, conclude  
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    ...  
}
```

_____ syscall (i.e. *kernel-userland*) interface

seL4 Microkit Library

seL4 OS Microkernel
Abstract Model

seL4 Microkit's assumptions need verifying!



```
static void handler_loop(void) { ...  
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    // if Q => S, conclude  
    {{ S }}  
    ...  
}
```

syscall (i.e. *kernel-userland*) interface

definition call_kernel :: "event $\Rightarrow$ (unit, ...) s_monad" **where**

```
call_kernel ev  $\equiv$  do  
    handle_event ev ...;  
    schedule;  
    activate_thread  
od
```

seL4 Microkit Library

seL4 OS Microkernel
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```
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od  
{{ Q }} ?
```

seL4 Microkit Library

seL4 OS Microkernel
Abstract Model

seL4 Microkit's assumptions need verifying!



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  {{ Q }}  
  // if Q => S, conclude  
  {{ S }}  
  ...  
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```

syscall (i.e. kernel-userland) interface

definition call_kernel :: "event $\Rightarrow$ (unit, ...) s_monad" **where**

{{ P }} {{ invs }}

call_kernel ev $\equiv$ do
 handle_event ev ...;
 schedule;
 activate_thread

od

{{ Q }} ? {{ invs }} incl. "doesn't crash"



seL4 Microkit Library

seL4 OS Microkernel
Abstract Model

seL4 Microkit's assumptions need verifying!



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static void handler_loop(void) { ...  
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  schedule;  
  activate_thread  
od  
{{ Q }} ?
```

Question:

Is proving a Hoare triple over one
call_kernel entry always enough?

seL4 Microkit Library

seL4 OS Microkernel
Abstract Model

seL4 Microkit's assumptions need verifying!



```
static void handler_loop(void) { ...
  {{ R && ! have_reply && ! microkit_have_signal }}
  // if R && ... => P, assume
  {{ P }}
  tag = seL4_Recv(INPUT_CAP, &badge, REPLY_CAP);
  {{ Q }}
  // if Q => S, conclude
  {{ S }}
  ...
}
```

syscall (i.e. kernel-userland) interface

definition call_kernel :: "event $\Rightarrow$ (unit, ...) s_monad" **where**

```
{{ P }}
call_kernel ev  $\equiv$  do
  handle_event ev ...;
  schedule;
  activate_thread
od
```

```
{{ Q }} ? X
```

Question:

Is proving a Hoare triple over one call_kernel entry always enough?

No.

seL4 Microkit Library

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Process A

```
static void handler_loop(void) { ...  
    {{ R && ... }}  
    // if R && ... => P, assume  
    {{ PA }}  
    tag = seL4_Recv(...);  
    {{ QA }}  
    // if Q => S, conclude  
    {{ S }}  
    ...  
}
```

seL4 Microkit Library

syscall (i.e. *kernel-userland*)
interface

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
    call_kernel ev ≡ do  
        handle_event ev ...;  
        schedule;  
        activate_thread
```

```
    od  
    {{ QA }} = {{ Q' && ... }}
```

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Process A

```
static void handler_loop(void) { ...  
    {{ R && ... }}  
    // if R && ... => P, assume  
    {{ PA }}  
    tag = seL4_Recv(...);  
    {{ QA }}  
    // if Q => S, conclude  
    {{ S }}  
    ...  
}
```

Process B

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
    call_kernel ev ≡ do  
        handle_event ev ...;  
        schedule;  
        activate_thread // B  
    od  
    {{ Q' && ... }}
```

seL4 Microkit Library

syscall (i.e. kernel–userland)
interface

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Process A

```
static void handler_loop(void) { ...  
    {{ R && ... }}  
    // if R && ... => P, assume  
    {{ PA }}  
    tag = seL4_Recv(...);  
    {{ QA }}  
    // if Q => S, conclude  
    {{ S }}  
    ...  
}
```

Process B

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
call_kernel ev ≡ do  
    handle_event ev ...;  
    schedule;  
    activate_thread // B  
od  
{{ Q' && ... }}
```

Unblocking seL4_Signal call

syscall (i.e. kernel–userland)
interface

seL4 OS Microkernel
Abstract Model

seL4 Microkit Library

seL4 System calls can block



Process A

```
static void handler_loop(void) { ...  
    {{ R && ... }}  
    // if R && ... => P, assume  
    {{ PA }}  
    tag = seL4_Recv(...);  
    {{ QA }}  
    // if Q => S, conclude  
    {{ S }}  
    ...  
}
```

Process B

```
static inline void  
microkit_notify(microkit_channel ch) { ...  
    {{ PB }}  
    seL4_Signal(... + ch);  
    {{ QB }}  
}
```

seL4 Microkit Library

syscall (i.e. kernel-userland)
interface

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
call_kernel ev ≡ do  
    handle_event ev ...;  
    schedule;  
    activate_thread // B  
od  
{{ Q' && ... }}
```

Unblocking seL4_Signal call

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Verifying these is
an unsolved problem*

Process A

```
static void handler_loop(void) { ...  
    {{ R && ... }}  
    // if R && ... => P, assume  
    {{ PA }}  
    tag = seL4_Recv(...);  
    {{ QA }}  
    // if Q => S, conclude  
    {{ S }}  
    ...  
}
```

Process B

```
static inline void  
microkit_notify(microkit_channel ch) { ...  
    {{ PB }}  
    seL4_Signal(... + ch);  
    {{ QB }}  
}
```

seL4 Microkit Library

* to the best of our knowledge, and
when they block on other processes
(not just I/O!)

syscall (i.e. *kernel-userland*)
interface

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
call_kernel ev ≡ do  
    handle_event ev ...;  
    schedule;  
    activate_thread // B  
od  
{{ Q' && ... }}
```

Unblocking seL4_Signal call

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Verifying these is
an unsolved problem*

Process A

```
static void handler_loop(void) { ...  
  {{ R && ... }}  
  // if R && ... => P, assume  
  {{ PA }}  
  tag = seL4_Recv(...);  
  {{ QA }}  
  // if Q => S, conclude  
  {{ S }}  
  ...  
}
```

Process B

```
static inline void  
microkit_notify(microkit_channel ch) { ...  
  {{ PB }}  
  seL4_Signal(... + ch);  
  {{ QB }}  
}
```

seL4 Microkit Library

* to the best of our knowledge, and
when they block on other processes
(not just I/O!)

syscall (i.e. *kernel-userland*)
interface

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  schedule;  
  activate_thread // B  
od  
{{ Q' && ... }}
```

Unblocking seL4_Signal call

```
{{ PB }} => {{ P'' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  schedule;  
  activate_thread  
od  
{{ Q'' && ... }}
```

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Verifying these is
an unsolved problem*

Process A

```
static void handler_loop(void) { ...  
  {{ R && ... }}  
  // if R && ... => P, assume  
  {{ PA }}  
  tag = seL4_Recv(...);  
  {{ QA }}  
  // if Q => S, conclude  
  {{ S }}  
  ...  
}
```

Process B

```
static inline void  
microkit_notify(microkit_channel ch) { ...  
  {{ PB }}  
  seL4_Signal(... + ch);  
  {{ QB }}  
}
```

seL4 Microkit Library

* to the best of our knowledge, and
when they block on other processes
(not just I/O!)

syscall (i.e. *kernel-userland*)
interface

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  schedule;  
  activate_thread // B  
od  
{{ Q' && ... }}
```

Unblocking seL4_Signal call

```
{{ PB }} => {{ P'' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  schedule;  
  activate_thread // A  
od  
{{ Q'' && ... }} => {{ QA }}
```

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Verifying these is
an unsolved problem*

Process A

```
static void handler_loop(void) { ...  
  {{ R && ... }}  
  // if R && ... => P, assume  
  {{ PA }}  
  tag = seL4_Recv(...);  
  {{ QA }}  
  // if Q => S, conclude  
  {{ S }}  
  ...  
}
```

Process B

```
static inline void  
microkit_notify(microkit_channel ch) { ...  
  {{ PB }}  
  seL4_Signal(... + ch);  
  {{ QB }}  
}
```

seL4 Microkit Library

* to the best of our knowledge, and
when they block on other processes
(not just I/O!)

syscall (i.e. *kernel-userland*)
interface

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  schedule;  
  activate_thread // B  
od  
{{ Q' && ... }}
```

Unblocking seL4_Signal call

```
{{ PB }} => {{ P'' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  schedule;  
  activate_thread // A  
od  
{{ Q'' && ... }} => {{ QA }}
```

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Verifying these is
an unsolved problem*

Process A

```
static void handler_loop(void) { ...  
  {{ R && ... }}  
  // if R && ... => P, assume  
  {{ PA }}  
  tag = seL4_Recv(...);  
  {{ QA }}  
  // if Q => S, conclude  
  {{ S }}  
  ...  
}
```

Process B

```
static inline void  
microkit_notify(microkit_channel ch) { ...  
  {{ PB }}  
  seL4_Signal(... + ch);  
  {{ QB }}  
}
```

seL4 Microkit Library

* to the best of our knowledge, and
when they block on other processes
(not just I/O!)

syscall (i.e. *kernel-userland*)
interface

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  ? schedule;  
  activate_thread // X  
od  
{{ Q' && ... }}
```

Unblocking seL4_Signal call

```
{{ PB }} => {{ P'' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  schedule;  
  activate_thread // A  
od  
{{ Q'' && ... }} => {{ QA }}
```

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Verifying these is
an unsolved problem*

Process A

```
static void handler_loop(void) { ...  
  {{ R && ... }}  
  // if R && ... => P, assume  
  {{ PA }}  
  tag = seL4_Recv(...);  
  {{ QA }}  
  // if Q => S, conclude  
  {{ S }}  
  ...  
}
```

Process B

```
static inline void  
microkit_notify(microkit_channel ch) { ...  
  {{ PB }}  
  seL4_Signal(... + ch);  
  {{ QB }}  
}
```

seL4 Microkit Library

* to the best of our knowledge, and
when they block on other processes
(not just I/O!)

syscall (i.e. *kernel-userland*)
interface

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  ? schedule;  
  activate_thread // X  
od  
{{ Q' && ... }}
```

Unblocking seL4_Signal call

```
{{ PB }} => {{ P'' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  schedule;  
  activate_thread // A  
od  
{{ Q'' && ... }} => {{ QA }}
```

⚡⚡⚡ X, Y, Z ... B

seL4 OS Microkernel
Abstract Model

seL4 System calls can block



Verifying these is
an unsolved problem*

Process A

```
static void handler_loop(void) { ...  
  {{ R && ... }}  
  // if R && ... => P, assume  
  {{ PA }}  
  tag = seL4_Recv(...);  
  {{ QA }}  
  // if Q => S, conclude  
  {{ S }}  
  ...  
}
```

Process B

```
static inline void  
microkit_notify(microkit_channel ch) { ...  
  {{ PB }}  
  seL4_Signal(... + ch);  
  {{ QB }}  
}
```

seL4 Microkit Library

* to the best of our knowledge, and
when they block on other processes
(not just I/O!)

syscall (i.e. *kernel-userland*)
interface

Blocking seL4_Recv call

```
{{ PA }} => {{ P' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  ? schedule;  
  activate_thread // X  
od  
{{ Q' && ... }}
```

Unblocking seL4_Signal call

```
{{ PB }} => {{ P'' && ... }}  
call_kernel ev ≡ do  
  handle_event ev ...;  
  schedule;  
  activate_thread // A  
od  
{{ Q'' && ... }} => {{ QA }}
```

⚡⚡⚡
X, Y, Z ... B
Irrelevant
calls
(IRQs too!)

seL4 OS Microkernel
Abstract Model

seL4 Towards kernel–userland functional proofs



Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \}$ seL4_Recv $\{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \}$ seL4_Signal $\{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

$\{\{ P \} \}$
call_kernel
 $\{\{ Q \} \}$

$\{\{ P' \} \}$
call_kernel
 $\{\{ Q' \} \}$

syscall (i.e. *kernel–userland*) interface

seL4 OS Microkernel
Abstract Model

seL4 Towards kernel–userland functional proofs



- It helps Microkit's assumptions are on *per-process* projections of kernel state:

Read:
ks_of = “kernel state of”

Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \} \text{seL4_Recv } \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{seL4_Signal } \{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

syscall (i.e. *kernel–userland*) interface

$\{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q \ (\text{ks_of } A \ s) \} \}$

$\{\{ \lambda s. P' \ (\text{ks_of } B \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$

seL4 OS Microkernel
Abstract Model

$\text{ks_of } p \ s \equiv \langle$
thread_cnode p s,
bound_notification p s,
mapped_writable p s,
not_writable_others p s,
recv_oracle s (bound_notification p s) (thread_cnode p s),
 $\lambda \text{ch. ntf_status } s \ (\text{thread_cnode } p \ s) \ \text{ch}$
 $\rangle$

seL4 Towards kernel–userland functional proofs



- It helps Microkit's assumptions are on *per-process* projections of kernel state:

Read:
ks_of = "kernel state of"

Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \} \text{ seL4_Recv } \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{ seL4_Signal } \{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

syscall (i.e. *kernel–userland*) interface

$\{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q \ (\text{ks_of } A \ s) \} \}$

$\{\{ \lambda s. P' \ (\text{ks_of } B \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$

seL4 OS Microkernel
Abstract Model

- On Microkit systems,
no $X \neq Y$ should possess the *capabilities*
to change **most parts** of (ks_of Y s).

ks_of p s $\equiv$ {
thread_cnode p s,
bound_notification p s, } cap state, thread init!
mapped_writable p s,
not_writable_others p s, } memory mappings!
recv_oracle s (bound_notification p s) (thread_cnode p s),
 $\lambda \text{ch. ntf_status } s \ (\text{thread_cnode } p \ s) \ \text{ch}$
}

seL4 Towards kernel–userland functional proofs



- It helps Microkit's assumptions are on *per-process* projections of kernel state:

Read:
ks_of = "kernel state of"

Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \} \text{ seL4_Recv } \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{ seL4_Signal } \{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

syscall (i.e. kernel–userland) interface

$\{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q \ (\text{ks_of } A \ s) \} \}$

$\{\{ \lambda s. P' \ (\text{ks_of } B \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$

seL4 OS Microkernel
Abstract Model

- On Microkit systems,
no $X \neq Y$ should possess the *capabilities*
to change **most parts** of (ks_of Y s).
- But we still have to prove that
the assumed changes happen.

$\text{ks_of } p \ s \equiv \{$
 $\left. \begin{array}{l} \text{thread_cnode } p \ s, \\ \text{bound_notification } p \ s, \\ \text{mapped_writable } p \ s, \\ \text{not_writable_others } p \ s, \end{array} \right\} \begin{array}{l} \text{cap state, thread init!} \\ \text{memory mappings!} \end{array}$
 $\text{recv_oracle } s \ (\text{bound_notification } p \ s) \ (\text{thread_cnode } p \ s),$
 $\lambda \text{ch. ntf_status } s \ (\text{thread_cnode } p \ s) \ \text{ch}$
 $\}$

seL4 What we're doing



- Defined state projections

Read:
ks_of = “kernel state of”

Thanks to



cyberagentur



Process A

$\{\{\lambda s. P\ s\}\} \text{seL4_Recv}\ \{\{\lambda s. Q\ s\}\}$

Process B

$\{\{\lambda s. P'\ s\}\} \text{seL4_Signal}\ \{\{\lambda s. Q'\ s\}\}$

seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

$\{\{\lambda s. P\ (ks_of\ A\ s)\}\}$
call_kernel
 $\{\{\lambda s. Q\ (ks_of\ A\ s)\}\}$

$\{\{\lambda s. P'\ (ks_of\ B\ s)\}\}$
call_kernel
 $\{\{\lambda s. Q'\ (ks_of\ B\ s)\}\}$

seL4 OS Microkernel
Abstract Model

Microkit-facing state

$ks_of\ p\ s\ :$

- thread_cnode p s,
- bound_notification p s, } **cap state, thread init!**
- mapped_writable p s,
- not_writable_others p s, } **memory mappings!**
- recv_oracle s (bound_notification p s) (thread_cnode p s),
- $\lambda ch. ntfn_status\ s\ (thread_cnode\ p\ s)\ ch$

seL4 What we're doing



- Defined state projections

Read:
ks_of = “kernel state of”

Thanks to



cyberagentur



Process A

$\{\{\lambda s. P\ s\}\} \text{seL4_Recv } \{\{\lambda s. Q\ s\}\}$

Process B

$\{\{\lambda s. P'\ s\}\} \text{seL4_Signal } \{\{\lambda s. Q'\ s\}\}$

seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

$\{\{\lambda s. P\ (ks_of\ A\ s)\}\}$
call_kernel
 $\{\{\lambda s. Q\ (ks_of\ A\ s)\}\}$

$\{\{\lambda s. P'\ (ks_of\ B\ s)\}\}$
call_kernel
 $\{\{\lambda s. Q'\ (ks_of\ B\ s)\}\}$

seL4 OS Microkernel
Abstract Model

Microkit-facing state

$ks_of\ p\ s$

Abstract Model state

- thread_cnode p s
 - bound_notification p s
 - mapped_writable p s
 - not_writable_others p s
 - recv_oracle s bound_notification p s (thread_cnode p s),
 - $\lambda ch. ntfn_status\ s\ (thread_cnode\ p\ s)\ ch$
- } cap state, thread init!
} memory mappings!

seL4 What we're doing



- Defined state projections
- Verifying Hoare triples on calls

Read:
ks_of = “kernel state of”

Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \} \text{seL4_Recv} \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{seL4_Signal} \{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

$\{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q \ (\text{ks_of } A \ s) \} \}$

$\{\{ \lambda s. P' \ (\text{ks_of } B \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$

seL4 OS Microkernel
Abstract Model

Abstract Model state

ks_of p s $\equiv$ (
 thread_cnode p s,
 bound_notification p s, } cap state, thread init!
 mapped_writable p s,
 not_writable_others p s, } memory mappings!
 recv_oracle s bound_notification p s) (thread_cnode p s),
 λch. ntfn_status s (thread_cnode p s) ch
)

seL4 What we're doing



- Defined state projections
- Verifying Hoare triples on calls

Read:
ks_of = “kernel state of”

Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \} \text{seL4_Recv} \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{seL4_Signal} \{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

$\{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q \ (\text{ks_of } A \ s) \} \}$

$\{\{ \lambda s. P' \ (\text{ks_of } B \ s) \} \}$
call_kernel
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$

seL4 OS Microkernel
Abstract Model

call_kernel ev $\equiv$ do
 handle_event ev ...;
 schedule;
 activate_thread
od

Abstract Model state

ks_of p s $\equiv$ (
 thread_cnode p s,
 bound_notification p s, } cap state, thread init!
 mapped_writable p s,
 not_writable_others p s, } memory mappings!
 recv_oracle s bound_notification p s) (thread_cnode p s),
 λch. ntfn_status s (thread_cnode p s) ch
)

seL4 What we're doing



- Defined state projections
- Verifying Hoare triples on calls

Read:
ks_of = “kernel state of”

Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \} \text{seL4_Recv} \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{seL4_Signal} \{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

$\{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$

call_kernel

$\{\{ \lambda s. Q \ (\text{ks_of } A \ s) \} \}$

$\{\{ \lambda s. P' \ (\text{ks_of } B \ s) \} \}$

call_kernel

$\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$

seL4 OS Microkernel
Abstract Model

```
call_kernel ev  $\equiv$  do
  handle_event ev ...;
  schedule;
  activate_thread } we'll come back to this
od
```

Abstract Model state

ks_of p s $\equiv$ (
 thread_cnode p s,
 bound_notification p s, } cap state, thread init!
 mapped_writable p s,
 not_writable_others p s, } memory mappings!
 recv_oracle s bound_notification p s) (thread_cnode p s),
 λ ch. ntfn_status s (thread_cnode p s) ch
)

seL4 What we're doing



- Defined state projections
- Verifying Hoare triples on calls

Read:
ks_of = “kernel state of”

Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \} \text{seL4_Recv} \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{seL4_Signal} \{\{ \lambda s. Q' \ s \} \}$

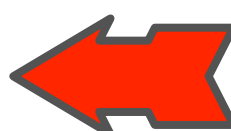
seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

$\{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$
handle_recv
 $\{\{ \lambda s. Q \ (\text{ks_of } A \ s) \} \}$

$\{\{ \lambda s. P' \ (\text{ks_of } B \ s) \} \}$
send_signal
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$

seL4 OS Microkernel
Abstract Model

call_kernel ev $\equiv$ do
 handle_event ev ...; 
 schedule;
 activate_thread } **we'll come back to this**
od

Abstract Model state
ks_of p s $\equiv$ (
 thread_cnode p s,
 bound_notification p s, } **cap state, thread init!**
 mapped_writable p s,
 not_writable_others p s, } **memory mappings!**
 recv_oracle s (bound_notification p s) (thread_cnode p s),
 λch. ntfn_status s (thread_cnode p s) ch
)

seL4 What we're doing



- Defined state projections
- Verifying Hoare triples on calls

Read:
ks_of = “kernel state of”

Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \} \text{seL4_Recv} \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{seL4_Signal} \{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

$\{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$
handle_recv
 $\{\{ \lambda s. Q \ (\text{ks_of } A \ s) \} \}$

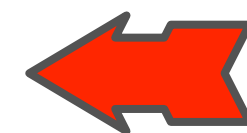


“Nonblocking”

$\{\{ \lambda s. P' \ (\text{ks_of } B \ s) \} \}$
send_signal
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$

seL4 OS Microkernel
Abstract Model

call_kernel ev $\equiv$ do
 handle_event ev ...;
 schedule;
 activate_thread } **we'll come back to this**
od



Abstract Model state

ks_of p s $\equiv$ (
 thread_cnode p s,
 bound_notification p s, } **cap state, thread init!**
 mapped_writable p s,
 not_writable_others p s, } **memory mappings!**
 recv_oracle s bound_notification p s) (thread_cnode p s),
 λch. ntfn_status s (thread_cnode p s) ch
)

seL4 What we're doing



- Defined state projections
- Verifying Hoare triples on calls

Read:
ks_of = “kernel state of”

Thanks to



cyberagentur



Process A

$\{\{ \lambda s. P \ s \} \} \text{seL4_Recv} \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{seL4_Signal} \{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

syscall (i.e. *kernel-userland*) interface

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 $\{\{ \lambda s. Q \ (ks_of \ A \ s) \} \}$ ✓ “Nonblocking”
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$\{\{ \lambda s. P' \ (ks_of \ B \ s) \} \}$
send_signal
 $\{\{ \lambda s. Q' \ (ks_of \ B \ s) \} \}$ ✓ **Blocking**
✓ **Unblocking**

seL4 OS Microkernel
Abstract Model

call_kernel ev $\equiv$ do
 handle_event ev ...;
 schedule;
 activate_thread } we'll come back to this
od

Abstract Model state
ks_of p s $\equiv$ (
 thread_cnode p s,
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seL4 OS Microkernel
Abstract Model

What we've proved:

- More precise cap lookup lemmas

$\text{ks_of } p \ s \equiv \{$
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seL4 OS Microkernel
Abstract Model

What we've proved:

- More precise cap lookup lemmas
- e.g. handle_recv, *as assumed*:
 - does not modify most ks_of fields

$ks_of \ p \ s \equiv \{$
 $\{ \text{thread_cnode } p \ s, \text{ bound_notification } p \ s, \}$ cap state, thread init!
 $\{ \text{mapped_writable } p \ s, \text{ not_writable_others } p \ s, \}$ memory mappings!
 recv_oracle s (bound_notification p s) (thread_cnode p s),
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seL4 What we're doing



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seL4 OS Microkernel
Abstract Model

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 - updates **ntfn_status** in Blocking case

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Thanks to



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seL4 OS Microkernel
Abstract Model

What we've proved:

- More precise cap lookup lemmas
- e.g. handle_recv, *as assumed*:
 - **does not modify** most ks_of fields
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- Lifting helpers for state projections

ks_of p s ≡ {

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seL4 What we're doing



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cyberagentur

Thanks to



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seL4 OS Microkernel
Abstract Model

- Proving & generalising their composition

seL4 What we're doing



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 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$ ✓ **Blocking**
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seL4 OS Microkernel
Abstract Model

- Proving & generalising their composition

$\{\{ \lambda s. P \ s \} \}$
seL4_SomeCall
 $\{\{ \lambda s. Q \ s \} \}$

seL4 What we're doing



- Defined state projections
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Read:
ks_of = “kernel state of”



cyberagentur

Thanks to



Process A

$\{\{ \lambda s. P \ s \} \} \text{seL4_Recv} \{\{ \lambda s. Q \ s \} \}$

Process B

$\{\{ \lambda s. P' \ s \} \} \text{seL4_Signal} \{\{ \lambda s. Q' \ s \} \}$

seL4 Microkit Library

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$\{\{ \lambda s. P' \ (\text{ks_of } B \ s) \} \}$
send_signal
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$ ✓ **Blocking**
✓ **Unblocking**

seL4 OS Microkernel
Abstract Model

- Proving & generalising their composition

$\{\{ \lambda s. P \ s \} \}$
seL4_SomeCall **Blocking A**
 $\{\{ \lambda s. Q \ s \} \}$

Unblocking B

seL4 What we're doing



- Defined state projections
- Verifying Hoare triples on calls

Read:
ks_of = “kernel state of”



cyberagentur

Thanks to



seL4 Microkit Library

Process A

$\{\{ \lambda s. P \ s \} \} \text{seL4_Recv} \{\{ \lambda s. Q \ s \} \}$

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$\{\{ \lambda s. P' \ s \} \} \text{seL4_Signal} \{\{ \lambda s. Q' \ s \} \}$

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send_signal
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$ ✓ **Blocking**
✓ **Unblocking**

seL4 OS Microkernel
Abstract Model

- Proving & generalising their composition

$\{\{ \lambda s. P \ s \} \}$
seL4_SomeCall
 $\{\{ \lambda s. Q \ s \} \}$ **Blocking A**

⚡⚡⚡ ⚡⚡⚡
C, D, E ... X, Y, Z
Irrelevant

Unblocking B

seL4 What we're doing



- Defined state projections
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Thanks to



Process A

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send_signal
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seL4 OS Microkernel
Abstract Model

- Proving & generalising their composition

$\{\{ \lambda s. P \ s \} \} \rightarrow \{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$
seL4_SomeCall **Blocking A**
 $\{\{ \lambda s. Q \ s \} \}$

⚡⚡⚡ ⚡⚡⚡
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Unblocking B

seL4 What we're doing



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seL4 Microkit Library

Process A

$\{\{ \lambda s. P \ s \} \} \text{ seL4_Recv } \{\{ \lambda s. Q \ s \} \}$

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$\{\{ \lambda s. P' \ s \} \} \text{ seL4_Signal } \{\{ \lambda s. Q' \ s \} \}$

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send_signal
 $\{\{ \lambda s. Q' \ (\text{ks_of } B \ s) \} \}$ ✓ **Blocking**
✓ **Unblocking**

seL4 OS Microkernel
Abstract Model

- Proving & generalising their composition

$\{\{ \lambda s. P \ s \} \} \xrightarrow{\text{seL4_SomeCall}} \{\{ \lambda s. P \ (\text{ks_of } A \ s) \} \}$
Blocking A
 $\{\{ \lambda s. Q \ s \} \} \quad \{\{ \lambda s. R \ (\text{ks_of } A \ s) \ \&\& \ P' \ (\text{ks_of } B \ s) \} \}$

⚡⚡⚡ ⚡⚡⚡
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Unblocking B

seL4 What we're doing



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cyberagentur

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seL4 Microkit Library

Process A

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seL4 OS Microkernel
Abstract Model

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⚡⚡⚡ ⚡⚡⚡
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$\{\{ \lambda s. R \ (\text{ks_of } A \ s) \ \&\& \ P' \ (\text{ks_of } B \ s) \} \}$
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seL4 OS Microkernel
Abstract Model

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seL4_SomeCall **Blocking A**
 $\{\{\lambda s. Q\ s\}\} \{\{\lambda s. R\ (\text{ks_of } A\ s)\} \ \&\& \ P'\ (\text{ks_of } B\ s)\}\}$



C, D, E ... X, Y, Z

Irrelevant

Note: If we can't prove these
irrelevant for wellformed Microkit systems,
then the seL4 kernel is incorrect!

$\{\{\lambda s. R\ (\text{ks_of } A\ s)\} \ \&\& \ P'\ (\text{ks_of } B\ s)\}\}$
Unblocking B

seL4 What we're doing



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seL4 OS Microkernel
Abstract Model

- Proving & generalising their composition

$\{\{\lambda s. P\ s\}\} \rightarrow \{\{\lambda s. P\ (ks_of\ A\ s)\}\}$
seL4_SomeCall **Blocking A**
 $\{\{\lambda s. Q\ s\}\} \quad \{\{\lambda s. R\ (ks_of\ A\ s)\ \&\&\ P'\ (ks_of\ B\ s)\}\}$



Note: If we can't prove these irrelevant for wellformed Microkit systems, then the seL4 kernel is incorrect!

$\{\{\lambda s. R\ (ks_of\ A\ s)\ \&\&\ P'\ (ks_of\ B\ s)\}\}$
Unblocking B
 $\{\{\lambda s. Q\ (ks_of\ A\ s)\ \&\&\ Q'\ (ks_of\ B\ s)\}\}$

seL4 What we're doing



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cyberagentur



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seL4 OS Microkernel
Abstract Model

- Proving & generalising their composition

$\{\{\lambda s. P\ s\}\} \rightarrow \{\{\lambda s. P\ (\text{ks_of } A\ s)\}\}$

Blocking A

seL4_SomeCall $\{\{\lambda s. R\ (\text{ks_of } A\ s)\ \&\&\ P'\ (\text{ks_of } B\ s)\}\}$



C, D, E ... X, Y, Z

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$\{\{\lambda s. R\ (\text{ks_of } A\ s)\ \&\&\ P'\ (\text{ks_of } B\ s)\}\}$

Unblocking B

$\{\{\lambda s. Q\ s\}\} \leftarrow \{\{\lambda s. Q\ (\text{ks_of } A\ s)\ \&\&\ Q'\ (\text{ks_of } B\ s)\}\}$

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C, D, E ... X, Y, Z

Irrelevant

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Unblocking B

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