



Limits to the efficiency of silicon multilayer thin film solar cells

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Abstract

Thin film crystalline silicon solar cells can only achieve high efficiencies if light trapping can be used to give a long optical path length, while simultaneously achieving near unity collection probabilities for all generated carriers. This necessitates a supporting substrate of a foreign material, with refractive index compatible with light trapping schemes for the silicon. The resulting inability to nucleate growth of crystalline silicon films of good crystallographic quality on such foreign substrates, at present, prevents the achievement of high efficiency devices using conventional single junction solar cell structures. The parallel multijunction solar cell provides a new approach for achieving high efficiencies from very poor quality material, with near unity collection probabilities for all generated carriers achieved through appropriate junction spacing. Heavy doping is used to minimise the dark saturation current contribution from the layers, therefore allowing respectable voltages. The design strategy, corresponding advantages, theoretical predictions and experimental results are presented.

1. Introduction

In the long term it is likely that thin film solar cells will displace bulk crystalline silicon devices for most applications [1]. The thin film technology that ultimately dominates will be dependent not only on cost but also on efficiency. It is unlikely that any photovoltaic technology will compete with conventional sources in grid-connected

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applications unless the photovoltaic module costs can be reduced to well below US\$1/W_p while simultaneously achieving efficiencies at least as high as present leading commercial technologies in the vicinity of 15% [2].

Considerable interest is now being shown worldwide in developing thin film crystalline silicon solar cell technologies [3]. Many years ago, crystalline silicon was discounted as being viable for thin film solar cells due to its relatively poor absorption. However, it is now well recognized that crystalline silicon's poor absorption is no longer an issue provided light trapping is introduced whereby the light is confined to regions where the photogenerated carriers have high collection probabilities. More specifically, an optical pathlength in excess of 100 microns with close to 100% internal quantum efficiencies for all generated carriers is probably essential to achieve the long term efficiency goal of 15% photovoltaic modules. This rules out the option of using low cost substrates of the same or similar refractive index to silicon due to the apparent inability to prevent large amounts of light penetrating into the non-active substrate material. Similarly, it appears unlikely that schemes relying on progressive enhancement of material quality through continued growth, with the device then formed into the uppermost (best quality) regions, will achieve the long term efficiency goals due to the same problem of light penetrating into non-active regions of the silicon.

The highest efficiency thin film crystalline silicon devices, whose design is potentially compatible with the implementation of light trapping (to confine the light to within regions where all the silicon is active), have been fabricated by Sanyo [4]. In these devices amorphous silicon is deposited onto a metal substrate and subsequently crystallised to give a thickness of 10 microns for the active material. Rather than a p-n junction being formed in the top surface, a heterojunction using another layer of amorphous silicon is used. Even though efficiencies to date are well below the long term goals, this approach appears to have considerable potential. However, much higher material quality in the crystallized silicon layer will be necessary.

An alternative approach that also appears capable of satisfying the above criteria but without the need for improved material quality is the multilayer multijunction solar cell [5]. The advantages of this new structure in comparison to conventional single junction structures will be described. Factors limiting the efficiencies will be identified, results to date summarized and ultimate performance predictions made.

2. Multilayer solar cells

Fig. 1 shows a schematic (not to scale) of the cross-section of a multilayer buried contact solar cell. The junctions are spaced so as to ensure carrier collection probabilities approach 100% throughout each layer, irrespective of material quality. An improved design criterion regarding layer dimensions, is to select the width of each so that the ratio of the current loss for each layer to its respective minority carrier diffusion length, is the same for all layers. The detrimental effects on current generation of high recombination velocities at the front and rear surfaces can be virtually eliminated through the use of very thin surface layers, preferably n-type for easier surface passivation. Lateral resistive losses in the surface layer can also be made negligible as

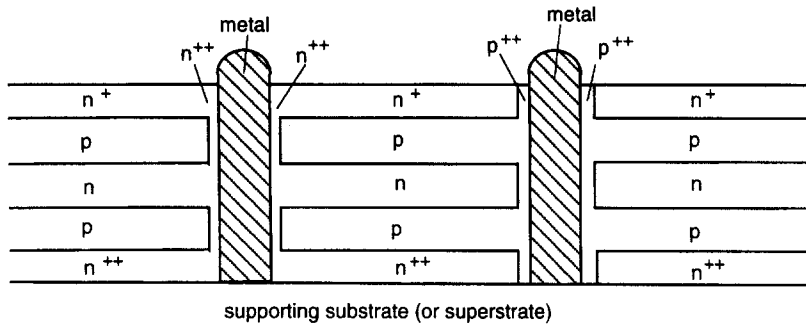


Fig. 1. Cross-section of a multilayer, parallel multijunction buried contact solar cell.

junction interaction facilitates the injection of majority carriers from the surface layer across the junction and into the underlying layer of opposite polarity where it diffuses as a minority carrier to the next underlying junction for collection. The buried contact approach neatly provides a means for contacting each of the underlying layers of the appropriate polarity. In addition, it retains the usual low cost, high efficiency attributes such as low metal shading, simultaneous electroless plating of both polarities of contacts, low metal resistive losses and high voltage capabilities by isolating the metal/silicon interface from the active device regions.

Low quality crystalline silicon layers such as those grown by Sanyo have their diffusion lengths limited primarily by crystal grain sizes and crystallographic quality rather than Auger recombination. Heavy doping of the silicon in the multilayer structure (typically 2–3 orders of magnitude greater than in conventional bulk devices) allows minimization of the dark saturation current while still achieving near unity internal quantum efficiencies for all wavelengths. In a 10 micron thick device, the heavy doping of the layers in conjunction with the junction interaction through carrier injection, provides extremely good lateral conductivity, sufficient to facilitate a spacing between adjacent metal fingers of the same polarity, approaching 1 cm.

2.1. External quantum efficiencies

Based on the device dimensions used by Sanyo [4], and similar material quality, a conventional single junction solar cell would be expected to have collection probabilities for carriers generated throughout the device, similar to those shown in the dotted curve in Fig. 2. This curve was derived assuming only moderate surface passivation, consistent with the expectations for low temperature growth processes. The corresponding internal quantum efficiencies are particularly poor for the short wavelength light due to the impact of the top surface, and longer wavelengths of light due to bulk and rear surface recombination. A good reflecting rear surface is assumed, to prevent rear surface absorption from having an impact on calculated internal quantum efficiencies.

In comparison, the introduction of additional collecting junctions facilitates the achievement of near unity collection probabilities for all carriers generated throughout the device, as shown in the solid curve in Fig. 2. Even the detrimental effects of the top

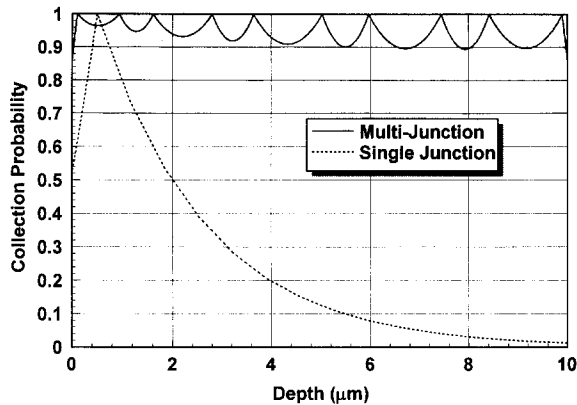


Fig. 2. Carrier collection probabilities for single junction and parallel multijunction devices, of 10 microns thickness with a corresponding defect lifetime of 10 ns. Surface recombination velocities are $2 \times 10^4 \text{ cm s}^{-1}$, while other modelling parameters are consistent with those used in PC-1D, other than the defect limited mobilities and inclusion of trap assisted tunnelling.

surface on current generation, can be virtually eliminated through the use of a very thin surface layer. This provides isolation for all carriers generated below the top junction, from the high top surface recombination velocity, therefore facilitating near unity internal quantum efficiencies even for very short wavelength light. A thin surface layer at the rear, although not as important as at the top surface, provides similar benefits. Therefore, the multilayer solar cell of Fig. 1 possesses high current generating capabilities, even with poor material quality and corresponding poor minority carrier diffusion lengths throughout the device.

Another related attribute of importance, is that these devices appear capable of tolerating much higher levels of contamination than conventional single junction devices. This is the case for two reasons. Firstly, the low effective minority carrier lifetimes, resulting from crystallographic defects and grain boundaries will remain virtually unaffected by quite large concentrations of unwanted contaminants such as gold, chromium, silver, etc. A detailed study of the impact of a large range of unwanted contaminants on the performance of multilayer multijunction solar cells, has been conducted and reported by Sproul et al. [6]. Secondly, even if contamination levels were sufficiently high to cause degradation of minority carrier diffusion lengths, the layer dimensions of the structure can be varied accordingly so as to still ensure near unity internal quantum efficiencies for all wavelengths of light. In fact, analysis shows that the poorer the material quality, the greater the advantage of the multi-layer structure of Fig. 1, over conventional single junction devices.

2.2. Open-circuit voltage

Poor minority carrier lifetimes will have an adverse effect on open-circuit voltage if the dark saturation current contribution from the bulk of the material exceeds the

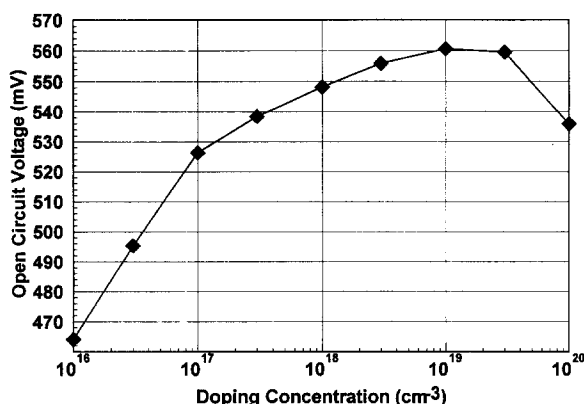


Fig. 3. Open-circuit voltage dependence on doping concentration for the multilayer device of Fig. 2 with the assumption of Lambertian light trapping and standard test conditions.

contribution from the surfaces. However, with defects and crystallographic imperfections limiting the minority carrier lifetimes, there is considerable scope for increasing the doping concentration to much higher levels than normally used in conventional bulk devices, without adversely affecting the minority carrier diffusion lengths. Since the dark saturation current contribution is directly dependent upon the minority carrier concentrations, the heavier doping acts to greatly reduce the dark saturation current contribution from the n- and p-type layers. Fig. 3 shows the dependence of the open-circuit voltage on the doping concentration within the layers, corresponding to a defect lifetime of 10 ns. The voltages were determined through the use of computer modelling programs, assuming Lambertian light trapping, 10 microns device thickness, and standard test conditions.

2.3. Resistive losses

One of the most interesting aspects of the multilayer multijunction device structure is its ability to minimise lateral resistance losses by injecting carriers between parallel layers. An extensive two-dimensional analysis of these effects has been conducted by Honsberg et al. [7]. For instance, the use of a very thin surface layer as described in Section 2.1, will have a very high lateral resistance, therefore making it unsuitable for the lateral conduction of all the carriers generated within it. The slightly higher voltage that therefore results across the top junction relative to the second junction, (when operating at maximum power point), will establish a concentration gradient of minority carriers in the p-type region that links the two junctions. Electrons consequently diffuse from the top junction to the second junction, with the higher minority carrier concentration near the top junction being maintained through the continued injection of electrons from the n-type layer into the p-type layer.

The effectiveness of this injection process is well demonstrated in Fig. 4, which shows the flow lines for the electron currents in a multijunction structure as determined through the use of the 2-D modelling program DESSIS [8]. Of particular relevance in

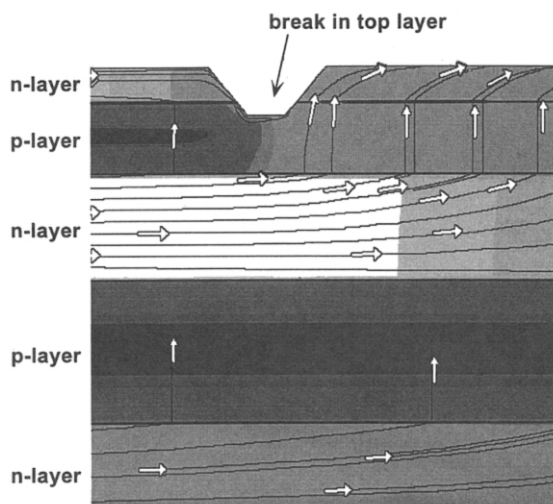


Fig. 4. Cross-section of a multilayer device showing flow lines for electron currents and corresponding electron current densities determined through the use of the 2-D modelling program DESSIS [8]. The discontinuity in the top n-type layer, forces large numbers of electrons to be injected to underlying n-type layers for lateral conduction.

this two dimensional modelling, is the discontinuity introduced into the top n-type layer forcing large numbers of electrons to be injected as shown to the underlying n-type layers for lateral conduction. Importantly, irrespective of the top layer sheet resistivity, the fill factor of the simulated device remains virtually unchanged. Clearly, the losses associated with these injection effects are dependent upon the relationship between the layer dimensions and the corresponding minority carrier diffusion lengths. The achievement of near unity internal quantum efficiencies as discussed in Section 2.1, guarantees the effectiveness of such injection processes.

A valuable consequence of the injection effects is that devices can be designed with very high lateral conductivities in underlying layers, therefore enabling the use of very widely spaced metal fingers. A typical design from the University of New South Wales, uses a spacing between the metal fingers of a given polarity of approximately 1 cm. This attribute provides for low metal shading losses, reduced contributions to the dark saturation current from the metal/silicon interface, and simplified processing.

2.4. Tolerance to grain boundaries

From the perspective of current collection, an active grain boundary will compete with nearby junctions for the collection of generated minority carriers. A commonly accepted guideline, is that the spacing between grain boundaries needs to be greater than the total device thickness to prevent excessive recombination and loss of short-circuit current. In comparison, with the multilayer structure of Fig. 1, the grain boundary spacing need only exceed the dimensions of the individual layers. The impact of both vertical and horizontal grain boundaries on both single junction and multi junction

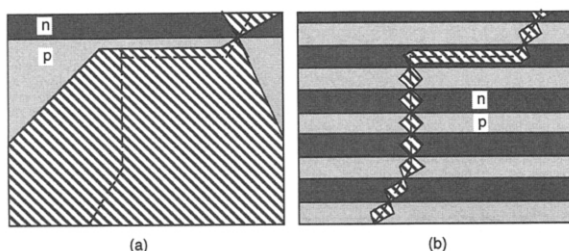


Fig. 5. Impact of vertical and horizontal grain boundaries on (a) single junction and (b) multilayer, parallel multijunction devices. Regions closer to grain boundaries than a junction are considered inactive and have, therefore, been shaded.

devices is illustrated in Fig. 5, in which all regions in closer proximity to a grain boundary than a junction are considered inactive and, therefore, shaded. Quite clearly the multijunction structure has far greater tolerance to grain boundaries in terms of current collection, than conventional single junction devices.

With regard to the impact of grain boundaries on device voltages, an analysis by Green [9] and Sproul et al. [6], shows that the nett effect of grain boundaries is equivalent to a region of reduced lifetime with correspondingly increased dark saturation current density.

2.5. Junction recombination

Due to the comparatively large junction area of multijunction devices in comparison to conventional single junction devices, junction recombination is of greater importance. For heavily doped material (such as that used in the multilayer devices), care needs to be exercised to avoid trap assisted tunnelling. This mechanism of recombination depends on the strength of the electric field and the presence of trap levels within the critical areas of the depletion region. Doping concentrations of 10^{18} cm^{-3} and higher, with a fairly abrupt junction between p- and n-type regions, provide the necessary conditions for this effect [10]. In multilayer devices, despite the heavy doping, this form of recombination can be avoided by appropriate grading of the doping concentrations in the junction region, which limits the maximum electric field strength.

The majority of the recombination in general occurs in only a small area of the depletion region, where the electron and hole concentrations are approximately equal (assuming equal capture cross sections). In reality, capture cross sections may vary significantly in which case the recombination will occur over a larger region. Through the use of junction engineering, it appears feasible to control doping concentrations and gradients so as to maximise the electric field strength in the areas of recombination, therefore effectively enhancing the carrier lifetimes. The extent to which this can be used to benefit, will be limited by trap assisted tunnelling.

To assist in improving the junction quality, it appears feasible for the first time in photovoltaic devices, to incorporate thin heavily doped layers (particularly phosphorus) in central regions, to enhance gettering of the unwanted contaminants and defects from

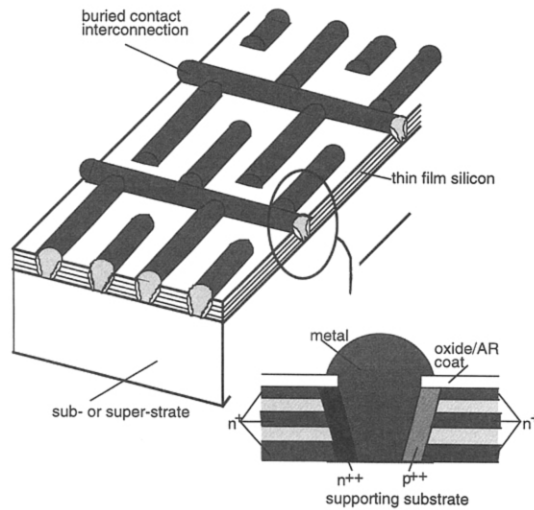


Fig. 6. Automatic series interconnection scheme for multilayer devices, whereby adjacent cells are series interconnected during the electroless plating. This is achieved through the use of overlapping, or very closely spaced n- and p-type grooves [11].

adjacent junctions. The flexibility associated with the design of multilayer devices also provides the option for varying the number of junctions and layer dimensions in response to the level of junction recombination experienced. Experimental devices to date have used relatively good quality material, therefore avoiding problems with junction recombination. A more detailed analysis of junction recombination, including the effects of grain boundaries, has been conducted by Green [9] and Sproul [6].

2.6. Automatic series interconnection during fabrication

By making the n-type busbar groove for one cell very close to the p-type busbar groove for the adjacent cell, the two regions can link during plating. This provides automatic series interconnection of adjacent cells during the electroless plating, therefore eliminating interconnects and subsequent soldering other than for the output leads. Perhaps the simplest implementation is shown in Fig. 6, where the described grooves actually overlap forming one wider groove with the two side walls oppositely doped. In this case, filling the groove with metal again automatically provides the series interconnection as shown.

2.7. Trading voltage for current

The heavy doping of the layers reduces their dark saturation contribution to well below the contributions from the surfaces and junctions. This facilitates the inclusion of a small concentration of lower bandgap material such as germanium, into one or more of

the layers without significant impact on the total device dark saturation current. The benefit results from the corresponding improved absorption achieved by the slight reduction in bandgap. The level of bandgap reduction and the thickness of the layer, can be controlled so as to limit the corresponding dark saturation current contribution to below the other major components in the device. With time, the quality of thin film crystalline silicon layers is expected to improve facilitating increased use of reduced bandgap material without adversely affecting voltages.

The concept of trading voltage for current is not new [9]. However, the common problems facing the inclusion of silicon alloys with reduced bandgap, include the difficulty in passivating surfaces and problems with junction recombination if the alloys penetrate into these regions. In the multilayer solar cell, not only can the dimensions of the layer incorporating the reduced bandgap alloy be carefully controlled, but it can also be isolated from the device surfaces through the use of isolating junctions on either side. The alloy can also be kept away from depletion regions, through control in the growth process.

Current improvement should result from the absorption of some wavelengths of light for which crystalline silicon is transparent, and the improved absorption of all other wavelengths of light normally absorbed by crystalline silicon. The importance of the latter is that it relaxes the requirements for good light trapping which has yet to be demonstrated as being experimentally feasible. However, the benefits of sub bandgap absorption, will not be as great as may be expected, due to free carrier absorption which increases significantly in heavily doped material.

Another approach for trading voltage for current is through the Impurity Photovoltaic Effect (IPV) which has been shown theoretically capable of enhancing device performance [12] through the deliberate inclusion of certain impurity types with energy levels within the bandgap (such as indium). The IPV effect could have particular importance in parallel multijunction devices for numerous reasons. Firstly, due to the anticipated poor material quality, relatively large quantities of, say, indium can be tolerated without degrading minority carrier lifetimes [6]. Secondly, if the impurity level lies in the lower half of the bandgap, then its inclusion in one of the heavily phosphorus doped n-type layers will ensure near 100% occupancy of the energy (trap) level. This enhances generation via these traps through the absorption of sub-bandgap photons that excite an electron from the trap level to the conduction band (a low probability process enhanced by high impurity concentration with corresponding high occupancy). Thirdly, the high occupancy greatly reduces the probability of the traps participating in two-step recombination processes. The net result is that generation via these traps can be made to greatly exceed the corresponding recombination. Fourthly, the flexibility in the growth processes for the multilayer structure facilitates the location of the desired impurities close to one or more junctions and if desired, with a corresponding gradient in the n-type dopant concentration to give field enhanced carrier lifetimes.

The IPV effect can therefore also be used to enhance absorption and corresponding current, particularly for sub-bandgap light, by trading voltage for current. However, the voltage loss through increased recombination is expected to be minimal and perhaps negative if the net generation rate via the traps exceeds the recombination rate at open-circuit.

3. Performance of multilayer solar cells

3.1. Fundamental efficiency limits

Fundamental efficiency limits for solar cells were shown by Shockley and Quiesser [13] to depend only on the semiconductor bandgap. However, a necessary assumption was that generated carriers have infinite mobilities and corresponding infinite diffusion lengths. For a conventional single junction device, these conditions are only approximated (even in good quality material) as the device thickness approaches zero. This is clearly not consistent with the requirement for light absorption.

The parallel multijunction structure of Fig. 1 provides an alternative approach for approximating infinite mobilities and diffusion lengths, while simultaneously satisfying the device thickness requirements for light trapping and absorption. Most importantly however, as actual carrier mobilities and diffusion lengths degrade with material quality, near unity internal quantum efficiencies (for all relevant wavelengths of light) can still be achieved by parallel multijunction devices.

3.2. Practical parallel multijunction devices

Extensive analysis of the multilayer solar cell has been conducted, with the predicted performance determined through two-dimensional modelling using the software package DESSIS. Efficiencies approaching 16% are predicted even with the use of material with only 10 ns lifetimes for the minority carriers. Experimental devices have been fabricated, with independently confirmed efficiencies in excess of 15% [14], using an inactive but good crystallographic quality single crystal silicon substrate onto which the multilayer structure was grown by chemical vapour deposition.

3.3. Device modelling

An interesting comparison is drawn between the world's most efficient silicon solar cell (the PERL Cell) and the multilayer solar cell, as a function of defect lifetime for the substrate material. In this analysis, the 10 micron thick multilayer cell has front and rear surface recombination velocities set at 20,000 cm/s, while for the PERL cell, a value of 1500 cm/s was used. Lambertian light trapping was assumed, while junction recombination was calculated using the model adopted by PC-1D. However, PC-1D does not allow for trap assisted tunnelling which has been included in this analysis in accordance with the model of Hurkx et al. [15]. The combination of optical losses (through reflection and shading) and resistive losses are set at 8% for the multijunction devices, and defect limited mobilities for minority carriers are included.

The results of the analysis are shown in Fig. 7, with the PERL cell having a very significant performance advantage with material that has a defect lifetime in the vicinity of 1 ms. However, with reducing defect lifetime, the multilayer cell performance remains approximately constant, as the collection probabilities for all generated carriers remain near unity, and the open-circuit voltage remains virtually unchanged due to the dominance of the surface effects in determining the total device dark saturation current.

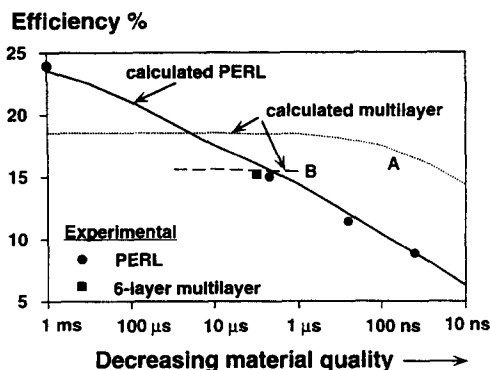


Fig. 7. Modelled and experimental curves for the PERL cell (highest efficiency silicon device), and a multilayer device, equivalent to the one modelled in Fig. 2, as a function of defect lifetime.

A small amount of degradation is evident for defect lifetimes of 10 ns, due to increasing junction recombination. In comparison, the PERL cell performance falls by approximately 75% for the same reduction in defect lifetime. Despite being the world's most efficient solar cell with good quality material, the predicted performance of the multilayer cell is more than 100% higher for a defect lifetime of 10 ns. An important aspect of these results is that the performance of a multilayer device demonstrated on good quality material also gives a good indication of the equivalent performance it will

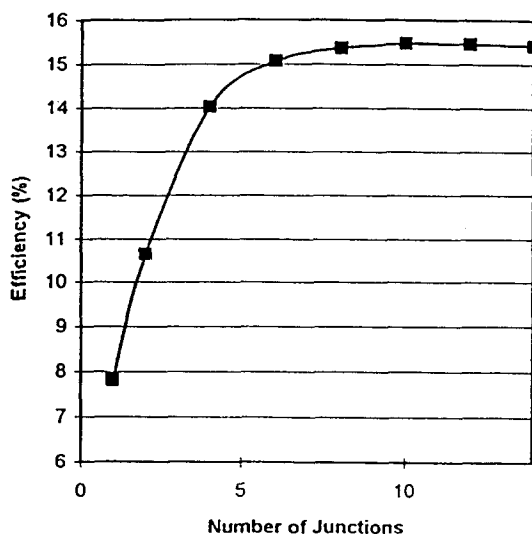


Fig. 8. Efficiency as a function of the number of junctions, for a 10 micron thick device, defect lifetime of 10 ns, and all other parameters as previously listed for the modelling in Figs. 2, 3, and 7. For each number of junctions, both the layer dimensions and the doping concentration were optimised to give the optimal design. Standard test conditions apply.

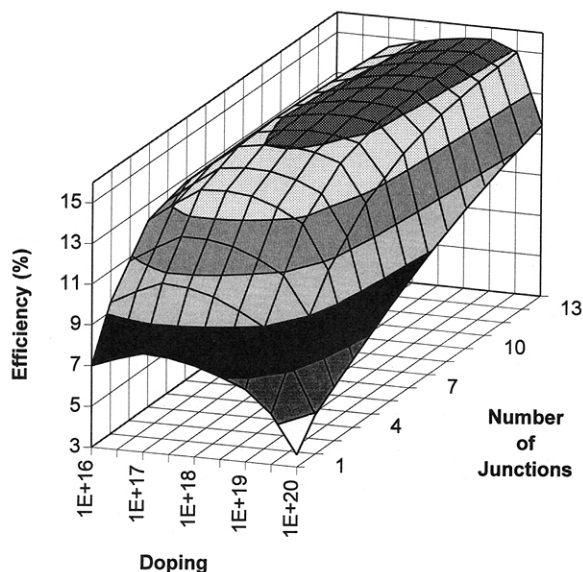


Fig. 9. Three dimensional plot showing contours of constant efficiency as a function of both doping concentration and the number of layers. The curve in Fig. 8 was extracted from the data comprising Fig. 9.

have on poor quality material. The results for experimental devices (multilayer and PERL cells) for various material qualities are presented by Green et al. [14].

For a 10 μm thick device, (the same thickness as used by Sanyo in demonstrating the present world record for a genuine thin film silicon solar cell on a foreign substrate), Fig. 8 shows the predicted efficiency as a function of the number of junctions. In this analysis, the defect lifetime was 10 ns, with all other parameters as listed above for the multilayer cell of Fig. 7. For each number of junctions, both the layer dimensions and the doping concentration were optimised to give the optimal design. It is interesting to note that a fairly broad maximum results for the optimum number of junctions as the additional current collected through extra junctions is offset by corresponding degradation in open-circuit voltage and fill factor as a result of increased junction recombination. More importantly, however, the performance for the multijunction devices is double that for a conventional single junction device. Fig. 9 shows the importance of doping concentrations to the results of Fig. 8, with the three-dimensional plot showing contours of constant efficiency as a function of both doping concentrations and the number of layers. Again, the dimensions for each layer are optimised for each combination of parameters in Fig. 9.

3.4. Experimental results

The experimental results achieved with the multilayer multijunction devices, are reported in the paper by Green et al. [14]. Efficiencies above 15% have been demonstrated, although as discussed above, have made use of inactive substrate material that

possesses excellent crystallographic qualities for the subsequent growth of the multilayer devices. The significance of these results, can be seen in the context of Fig. 7, where it was demonstrated that the performance of the multilayer devices are unlikely to change significantly with deteriorating material quality. On this basis, the demonstrated feasibility and performance of the multilayer devices on good crystallographic material is of significance for future generations of devices fabricated with poor quality material.

Photographs of experimental devices (cross-sections) comprising 6 layers grown by CVD and buried contacts, have been published by Sproul et al. [6].

4. Conclusions

The multilayer multijunction devices have many advantages over conventional single junction devices, particularly with lower quality crystalline silicon material. In the limit of extremely good quality material, single junction and multijunction device designs merge to a common performance level. However, the performance advantage of the multijunction devices increases continually as the material defect lifetime deteriorates. A detailed analysis has been used to demonstrate that, on material of similar dimensions and quality as used to fabricate the highest efficiency thin film devices on foreign substrates, multijunction devices can be expected to have efficiencies more than double those achieved by conventional single junction devices.

Similarly, the world's most efficient silicon solar cell (the PERL Cell) falls to well below the performance levels of the multijunction devices when the defect lifetimes in the material falls below about 10 μ s. Again, the performance advantage of the multijunction devices increases significantly with deteriorating defect lifetimes, with a performance advantage in excess of 100% for defect lifetimes of 10 ns.

The multilayer cells are able to achieve near unity internal quantum efficiencies for all wavelengths of light irrespective of the quality of the material and the quality of the surface passivation. Other attributes include: respectable voltages achieved through heavy doping; minimal resistive losses, with widely spaced fingers able to be accommodated by capitalising on injection effects through junction interaction; and superior tolerance to grain boundaries relative to conventional devices. The buried contact solar cell scheme, already well demonstrated through previous generations of technology, provides a neat and simple and low cost approach for contacting each of the horizontal layers of the appropriate polarity, while simultaneously providing the high efficiency attributes normally achieved by buried contact solar cells.

The limitations to device performance do not depend heavily on the defect lifetime of the material although indirectly, the defect lifetime through junction recombination will have an impact on the optimum number of junctions and, therefore, device thickness. The open-circuit voltages are expected to be limited by the surfaces, unless very poor defect lifetimes lead to junction recombination limiting this parameter. Currents are limited primarily by the optics of the device, with collection probabilities for the generated carriers throughout the device approaching unity, irrespective of the material quality. The fill factors will degrade with increasing junction recombination in response to deteriorating defect lifetimes, although this effect is somewhat camouflaged by a shift

in the optimal design to smaller numbers of junctions. Considerable scope for minimising junction recombination exists through junction engineering since the majority of recombination occurs within an extremely small volume where the carrier concentrations are approximately equal (assuming equal capture cross sections). The net result, is that modules approaching 15% efficiency should be feasible through the use of the multi-junction structure, even with material lifetimes as poor as 10 ns. Modules based on single junction devices and similar material quality, are unlikely to exceed half this efficiency.

Acknowledgements

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